

# **LINEAR AND DIGITAL IC APPLICATIONS**

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# Course Contents

- **Unit 1** - **Operational Amplifier**
- **Unit 2** - **OP-Amp, IC555 & IC565 Applications**
- **Unit 3** - **Data Converters**
- **Unit 4** - **Digital Integrated circuits**
- **Unit 5** - **Sequential Logic IC's & Memories**



## **Text Books:**

1. Linear Integrated Circuits – D. Roy Choudhury
2. Op-Amps & Linear ICs – Ramakanth A. Gayakwad.
3. Digital Fundamentals – Floyd and Jain



# Unit 1- Integrated Circuits

- What is an Integrated Circuit?
- Where do you use an Integrated Circuit?
- Why do you prefer an Integrated Circuit to the circuits made by interconnecting discrete components?

Def: The “Integrated Circuit “ or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon.



In 1958 Jack Kilby of Texas Instruments invented first IC



## Applications of an Integrated Circuit

- Communication
- Control
- Instrumentation
- Computer
- Electronics



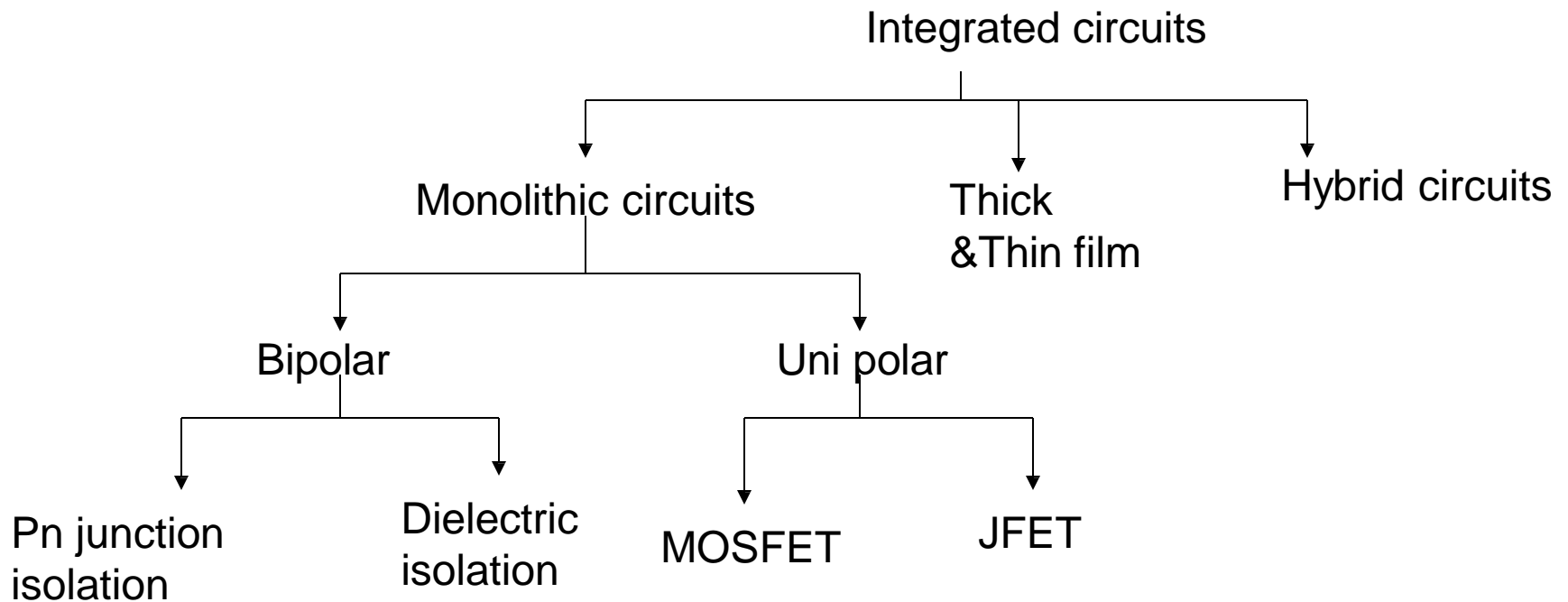
## Advantages:

- Small size
- Low cost
- Less weight
- Low supply voltages
- Low power consumption
- Highly reliable
- Matched devices
- Fast speed

# Classification



- Digital ICs
- Linear ICs



## Classification of ICs





# Chip size and Complexity

- Invention of Transistor (Ge) - 1947
- Development of Silicon - 1955-1959
- Silicon Planar Technology - 1959
- First ICs, SSI (3- 30gates/chip) - 1960
- MSI ( 30-300 gates/chip) - 1965-1970
- LSI ( 300-3000 gates/chip) -1970-1975
- VLSI (More than 3k gates/chip) - 1975
- ULSI (more than one million active devices are integrated on single chip)

<b>SSI</b>	<b>MSI</b>	<b>LSI</b>	<b>VLSI</b>	<b>ULSI</b>
< 100 active devices	100-1000 active devices	1000-100000 active devices	>100000 active devices	Over 1 million active devices
Integrated resistors, diodes & BJT's	BJT's and Enhanced MOSFETS	MOSFETS	8bit, 16bit Microprocessors	Pentium Microprocessors

## Selection of IC Package

Type	Criteria
Metal can package	<ol style="list-style-type: none"><li>1. Heat dissipation is important</li><li>2. For high power applications like power amplifiers, voltage regulators etc.</li></ol>
DIP	<ol style="list-style-type: none"><li>1. For experimental or bread boarding purposes as easy to mount</li><li>2. If bending or soldering of the leads is not required</li><li>3. Suitable for printed circuit boards as lead spacing is more</li></ol>
Flat pack	<ol style="list-style-type: none"><li>1. More reliability is required</li><li>2. Light in weight</li><li>3. Suited for airborne applications</li></ol>

# Factors affecting selection of IC package

- Relative cost
- Reliability
- Weight of the package
- Ease of fabrication
- Power to be dissipated
- Need of external heat sink



# Temperature Ranges

1. Military temperature range :  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $-55^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
2. Industrial temperature range :  $-20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
3. Commercial temperature range:  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  ( $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ )



# Operational Amplifier

**The operational amplifier (Op-Amp) is a multi-terminal device which internally is quite complex.**

# Operational Amplifier

An “Operational amplifier” is a direct coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and output stage.

The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.



## Basic Information of Op-Amp

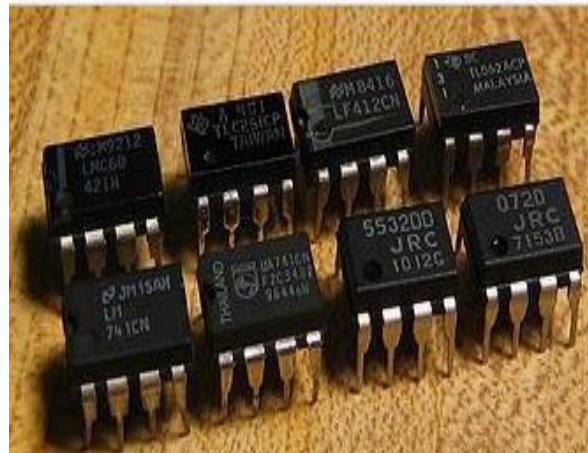
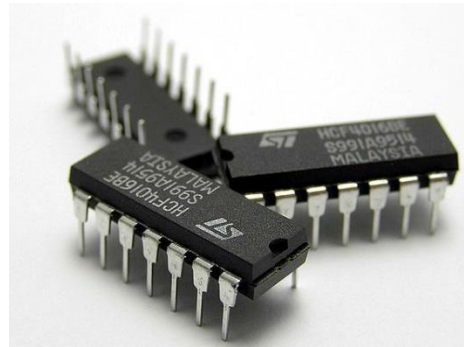
Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals.



# Packages



The metal can (TO)  
Package



The Dual-in-Line (DIP)  
Package



The Flat Package

# Basic Information of an Op-amp contd...

Power supply connection:

The power supply voltage may range from about  $\pm 5V$  to  $\pm 22V$ .

The common terminal of the  $V^+$  and  $V^-$  sources is connected to a reference point or ground.


# Manufacturer's Designation for Linear ICs

- Fairchild -  $\mu$ A,  $\mu$ AF
- National Semiconductor - LM, LH, LF, TBA
- Motorola - MC, MFC
- RCA - CA, CD
- Texas Instruments - SN
- Signetics - N/S, NE/SE
- Burr- Brown - BB



**Fairchild's original  $\mu$ A741 is also manufactured by other manufactures as follows**

- National Semiconductor - LM741
- Motorola - MC1741
- RCA - CA3741
- Texas Instruments - SN52741
- Signetics - N5741

- 
- **741**            **Military grade op-amp**
  - **741C**           **Commercial grade op-amp**
  - **741A**           **Improved version of 741**
  - **741E**           **Improved version of 741C**
  - **741S**           **Military grade op-amp with higher slew rate**
  - **741SC**        **Commercial grade op-amp with higher slew rate**

# Differential Amplifier

$$V_0 = A_d (V_1 - V_2)$$

$$A_d = 20 \log_{10} (A_d) \text{ in dB}$$

$$V_c = \frac{(V_1 + V_2)}{2}$$

$$\text{CMRR} = \rho = \left| \frac{A_d}{A_c} \right|^2$$

# Characteristics and performance parameters of Op-amp

- **Input offset Voltage**
- **Input offset current**
- **Input bias current**
- **Differential input resistance**
- **Input capacitance**
- **Open loop voltage gain**
- **CMRR**
- **Output voltage swing**

# Characteristics and performance parameters of Op-amp

- **Output resistance**
- **Offset adjustment range**
- **Input Voltage range**
- **Power supply rejection ratio**
- **Power consumption**
- **Slew rate**
- **Gain – Bandwidth product**
- **Equivalent input noise voltage and current**



# Characteristics and performance parameters of Op-amp

- Average temperature coefficient of offset parameters
- Output offset voltage
- Supply current

# 1. Input Offset Voltage

The differential voltage that must be applied between the two input terminals of an op-amp, to make the output voltage zero.

It is denoted as  $V_{ios}$

For op-amp 741C the input offset voltage is 6mV

## 2. Input offset current

The algebraic difference between the currents flowing into the two input terminals of the op-amp

**It is denoted as  $I_{ios} = |I_{b1} - I_{b2}|$**

For op-amp 741C the input offset current is 200nA

### 3. Input bias current

The average value of the two currents flowing into the op-amp input terminals

It is expressed mathematically as

$$\frac{I_{b1} + I_{b2}}{2}$$

For 741C the maximum value of  $I_b$  is 500nA

## 4. Differential Input Resistance

It is the equivalent resistance measured at either the inverting or non-inverting input terminal with the other input terminal grounded

**It is denoted as  $R_i$**

For 741C it is of the order of  $2M\Omega$

## 5. Input capacitance

It is the equivalent capacitance measured at either the inverting or non-inverting input terminal with the other input terminal grounded.

**It is denoted as  $C_i$**

For 741C it is of the 1-4 pF

## 6. Open loop Voltage gain

It is the ratio of output voltage to the differential input voltage, when op-amp is in open loop configuration, without any feedback. It is also called as large signal voltage gain

It is denoted as  $A_{OL}$   $A_{OL} = V_o / V_d$

For 741C it is typically 200,000

## 7. CMRR

It is the ratio of differential voltage gain  $A_d$  to common mode voltage gain  $A_c$

$$\text{CMRR} = A_d / A_c$$

$A_d$  is open loop voltage gain  $A_{OL}$  and  $A_c = V_{OC} / V_c$

For op-amp 741C CMRR is 90 dB



## 8. Output Voltage swing

The op-amp output voltage gets saturated at  $+V_{CC}$  and  $-V_{EE}$  and it cannot produce output voltage more than  $+V_{CC}$  and  $-V_{EE}$ . Practically voltages  $+V_{sat}$  and  $-V_{sat}$  are slightly less than  $+V_{CC}$  and  $-V_{EE}$ .

For op-amp 741C the saturation voltages are  $\pm 13V$  for supply voltages  $\pm 15V$

## 9. Output Resistance

It is the equivalent resistance measured between the output terminal of the op-amp and ground

It is denoted as  $R_o$

For op-amp 741 it is  $75\Omega$

## 10. Offset voltage adjustment range

The range for which input offset voltage can be adjusted using the potentiometer so as to reduce output to zero

For op-amp 741C it is  $\pm 15\text{mV}$

## 11. Input Voltage range

It is the range of common mode voltages which can be applied for which op-amp functions properly and given offset specifications apply for the op-amp

For  $\pm 15V$  supply voltages, the input voltage range is  $\pm 13V$

## 12. Power supply rejection ratio

PSRR is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping the other power supply voltage constant. It is also called as power supply sensitivity (PSV)

$$\text{PSRR} = (\Delta v_{\text{ios}} / \Delta V_{\text{cc}}) |_{\text{constant } V_{\text{EE}}}$$

$$\text{PSRR} = (\Delta v_{\text{ios}} / \Delta V_{\text{EE}}) |_{\text{constant } V_{\text{cc}}}$$

The typical value of PSRR for op-amp 741C is  $30\mu\text{V/V}$

## 13. Power Consumption

It is the amount of quiescent power to be consumed by op-amp with zero input voltage, for its proper functioning

It is denoted as  $P_c$

For 741C it is 85mW

## 14. Slew rate

It is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/ $\mu$ sec

$$\text{Slew rate} = S = dV_o / dt |_{\max}$$

It is specified by the op-amp in unity gain condition.

The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the internal stages of op-amp, when a high frequency large amplitude signal is applied.

## Slew rate

It is given by  $dV_c/dt = I/C$

For large charging rate, the capacitor should be small or the current should be large.

$$S = I_{\max} / C$$

For 741 IC the charging current is  $15 \mu\text{A}$  and the internal capacitor is  $30 \text{ pF}$ .  $S = 0.5\text{V}/\mu\text{sec}$



# Slew rate equation

$$V_s = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$

$$S = \text{slew rate} = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

$$S = V_m \omega = 2 \pi f V_m$$

$$S = 2 \pi f V_m \text{ V / sec}$$

This is also called **full power bandwidth** of the op-amp

For distortion free output, the maximum allowable input

frequency  $f_m$  can be obtained as

$$f_m = \frac{S}{2 \pi V_m}$$

## 15. Gain – Bandwidth product

It is the bandwidth of op-amp when voltage gain is unity (1).

It is denoted as GB.

The GB is also called unity gain bandwidth (UGB) or closed loop bandwidth

It is about 1MHz for op-amp 741C

## 16. Equivalent Input Noise Voltage and Current

The noise is expressed as a power density

Thus equivalent noise voltage is expressed as  $V^2/\text{Hz}$

while the equivalent noise current is expressed as  $A^2/\text{Hz}$

## 17. Average temperature coefficient of offset parameters

The average rate of change of input offset voltage per unit change in temperature is called average temperature coefficient of input offset voltage or input offset voltage drift

It is measured in  $\mu\text{V}/^\circ\text{C}$ . For 741 C it is  $0.5 \mu\text{V}/^\circ\text{C}$

The average rate of change of input offset current per unit change in temperature is called average temperature coefficient of input offset current or input offset current drift

It is measured in  $\text{nA}/^\circ\text{C}$  or  $\text{pA}/^\circ\text{C}$  . For 741 C it is  $12 \text{pA}/^\circ\text{C}$

## 18. Output offset voltage ( $V_{oos}$ )

The output offset voltage is the dc voltage present at the output terminals when both the input terminals are grounded.

It is denoted as  $V_{oos}$

# Factors affecting parameters of Op-amp

Supply Voltage

1. Voltage gain
2. Output Voltage swing
3. Input voltage range
4. Power consumption
5. Input offset current

Frequency

1. Voltage gain
2. Input resistance
3. Output resistance
4. CMRR
5. Input noise voltage
6. Input noise current

Temperature

1. Input offset current
2. Input offset voltage
3. Input bias current
4. Power consumption
5. Gain-Bandwidth product
6. Slew rate
7. Input resistance

# Parameter consideration for various applications

<b>For A.C. applications</b>	<b>For D.C. applications</b>
Input resistance	Input resistance
Output resistance	Output resistance
Open loop voltage gain	Open loop voltage gain
Slew rate	Input offset voltage
Output voltage swing	Input offset current
Gain- bandwidth product	Input offset voltage and current drifts
Input noise voltage and current	
Input offset voltage and current drifts	

# Absolute Maximum Ratings of Op-amp

- **Maximum power dissipation:** This is the maximum power which can be dissipated, in the internal stages of the op-amp in the form of heat
- **Operating temperature range:** As specified in the data sheet, op-amp can work satisfactorily, over the operating temperature range, as required for the given application



# Absolute Maximum Ratings of Op-amp

- **Maximum supply voltage:** This is the maximum d.c. supply voltage which can be applied to the op-amp
- **Maximum differential input voltage:** This rating gives the maximum value of difference between the two input voltages, applied to the two input terminals of the op-amp

# Absolute Maximum Ratings of Op-amp

- **Maximum common mode input voltage:** This is the maximum value of the input voltage which can be simultaneously applied to the two input terminals
- **Storage temperature range:** This gives the temperature range over which the op-amp can be stored safely.



# Op-amp characteristics dependent on the power supply voltages

- Absolute maximum power supply voltage
- Absolute maximum differential input voltages
- Absolute maximum common mode input voltage

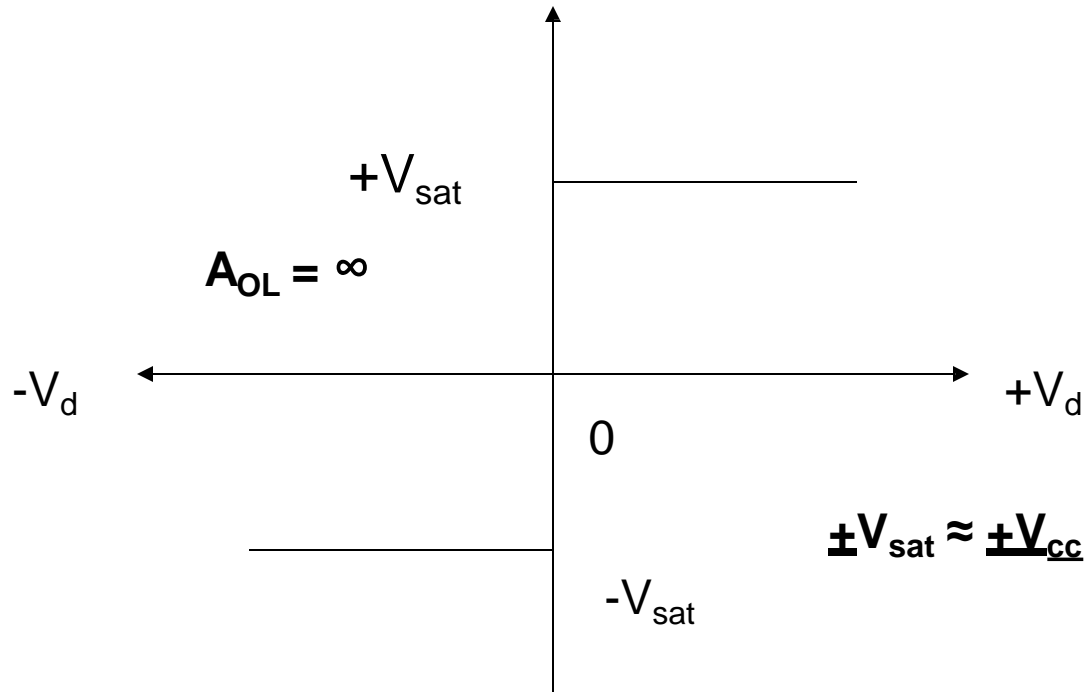
# Ideal Op-amp

1. An ideal op-amp draws no current at both the input terminals  
i.e.  $I_1 = I_2 = 0$ . Thus its input impedance is infinite. Any source can drive it and there is no loading
2. The gain of an ideal op-amp is infinite, hence the differential input  $V_d = V_1 - V_2$  is essentially zero for the finite output voltage  $V_o$   
on the driver stage
3. The output voltage  $V_o$  is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits

# The Ideal Operational Amplifier

- Open loop voltage gain  $A_{OL} = \infty$
- Input Impedance  $R_i = \infty$
- Output Impedance  $R_o = 0$
- Bandwidth  $BW = \infty$
- Zero offset ( $V_o = 0$  when  $V_1 = V_2 = 0$ )  $V_{ios} = 0$
- CMRR  $\rho = \infty$
- Slew rate  $S = \infty$
- No effect of temperature
- Power supply rejection ratio  $PSRR = 0$

# Ideal Voltage transfer curve



## Practical voltage transfer curve

1. If  $V_d$  is greater than corresponding to b, the output attains  $+V_{sat}$
2. If  $V_d$  is less than corresponding to a, the output attains  $-V_{sat}$
3. Thus range a-b is input range for which output varies linearly with the input. But  $A_{OL}$  is very high, practically  
this range is very small

# Equivalent circuit of practical op-amp

$A_{OL}$  = Large signal open loop voltage gain

$V_d$  = Difference voltage  $V_1 - V_2$

$V_1$  = Non-inverting input voltage with respect to ground

$V_2$  = Inverting input voltage with respect to ground

$R_i$  = Input resistance of op-amp

$R_o$  = Output resistance of op-amp



## Transient Response Rise time

When the output of the op-amp is suddenly changing like pulse type, then the rise time of the response depends on the cut-off frequency  $f_H$  of the op-amp. Such a rise time is called cut-off frequency limited rise time or transient response rise time ( $t_r$ )

$$t_r = \frac{0.35}{f_H}$$

# Op-amp Characteristics

## ■ DC Characteristics

Input bias current Input offset current Input  
offset voltage Thermal drift

## ■ AC Characteristics

Slew rate Frequency response

## DC Characteristics Thermal Drift

The op-amp parameters input offset voltage  $V_{ios}$  and input offset current  $I_{ios}$  are not constants but vary with the factors

1. Temperature
2. Supply Voltage changes
3. Time

# Thermal Voltage Drift

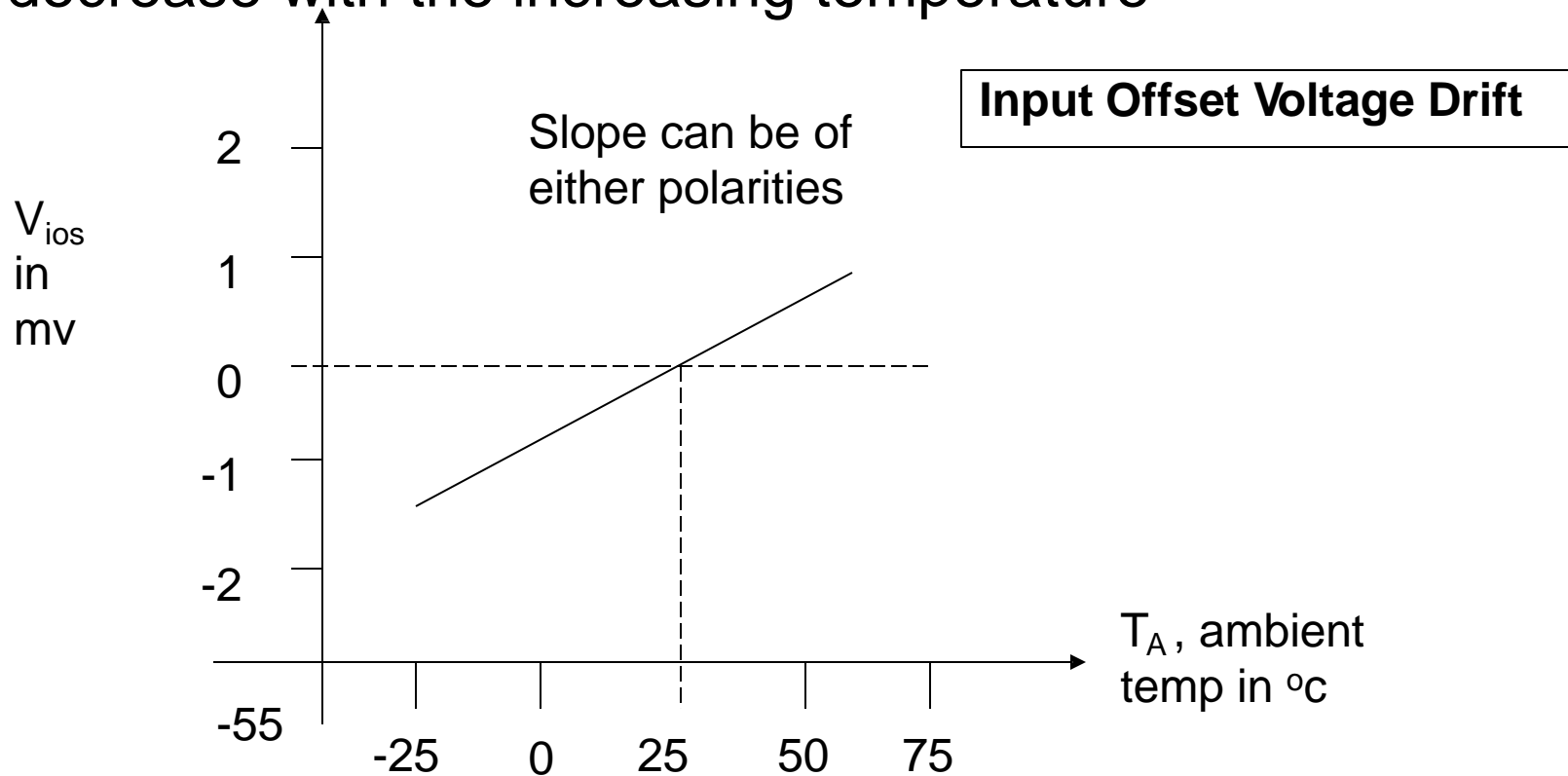
It is defined as the average rate of change of input offset voltage per unit change in temperature. It is also called as input offset voltage drift

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

$\Delta V_{ios}$  = change in input offset voltage

$\Delta T$  = Change in temperature

It is expressed in  $\mu\text{V}/^\circ\text{C}$ . The drift is not constant and it is not uniform over specified operating temperature range. The value of input offset voltage may increase or decrease with the increasing temperature



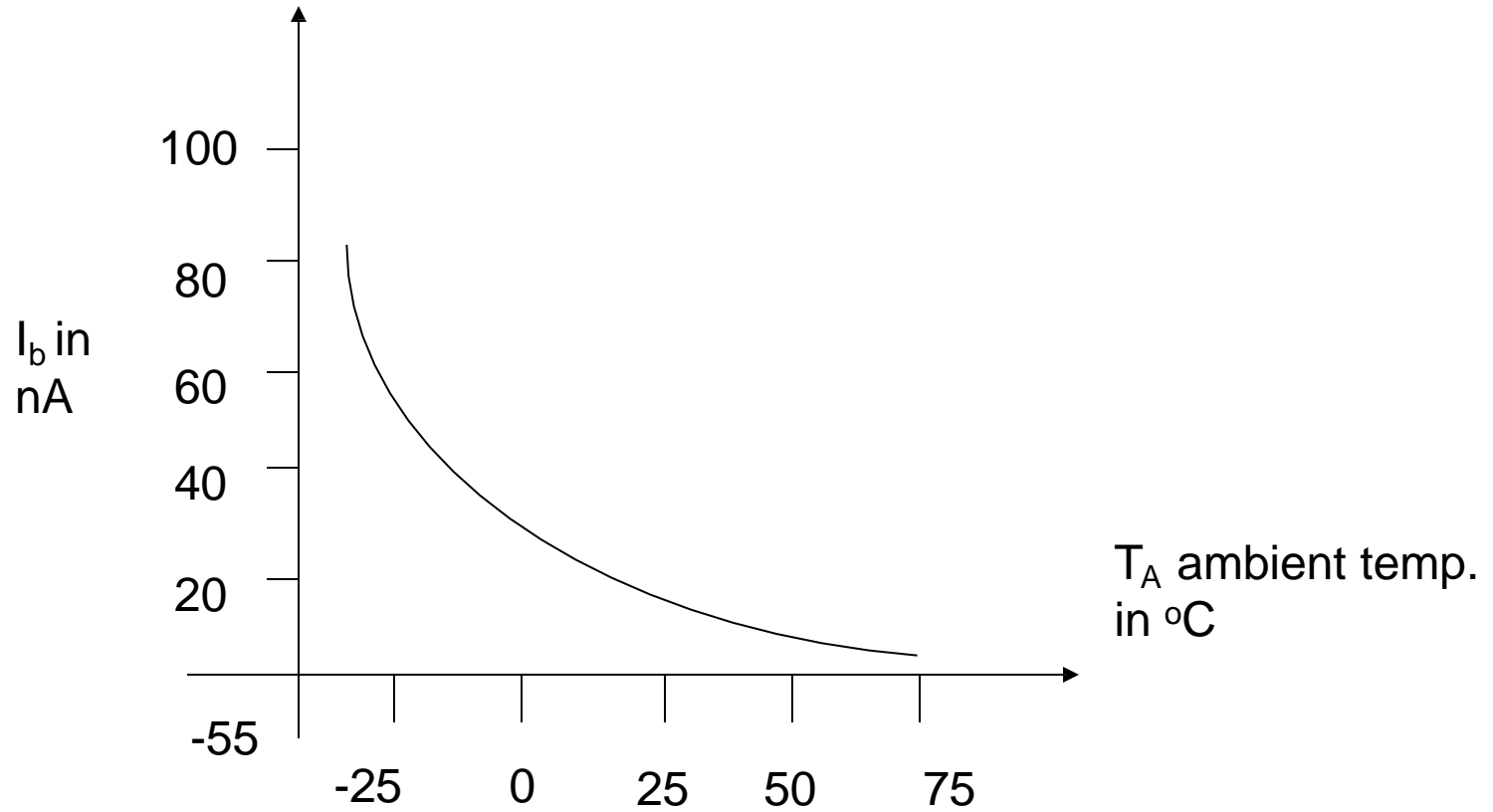
## Input bias current drift

It is defined as the average rate of change of input bias current per unit change in temperature

$$\text{Thermal drift in input bias current} = \frac{\Delta I_b}{\Delta T}$$

It is measured in nA/°C or pA/°c. These parameters vary randomly with temperature. i.e. they may be positive in one temperature range and negative in another

## Input bias current drift



# Input Offset current drift

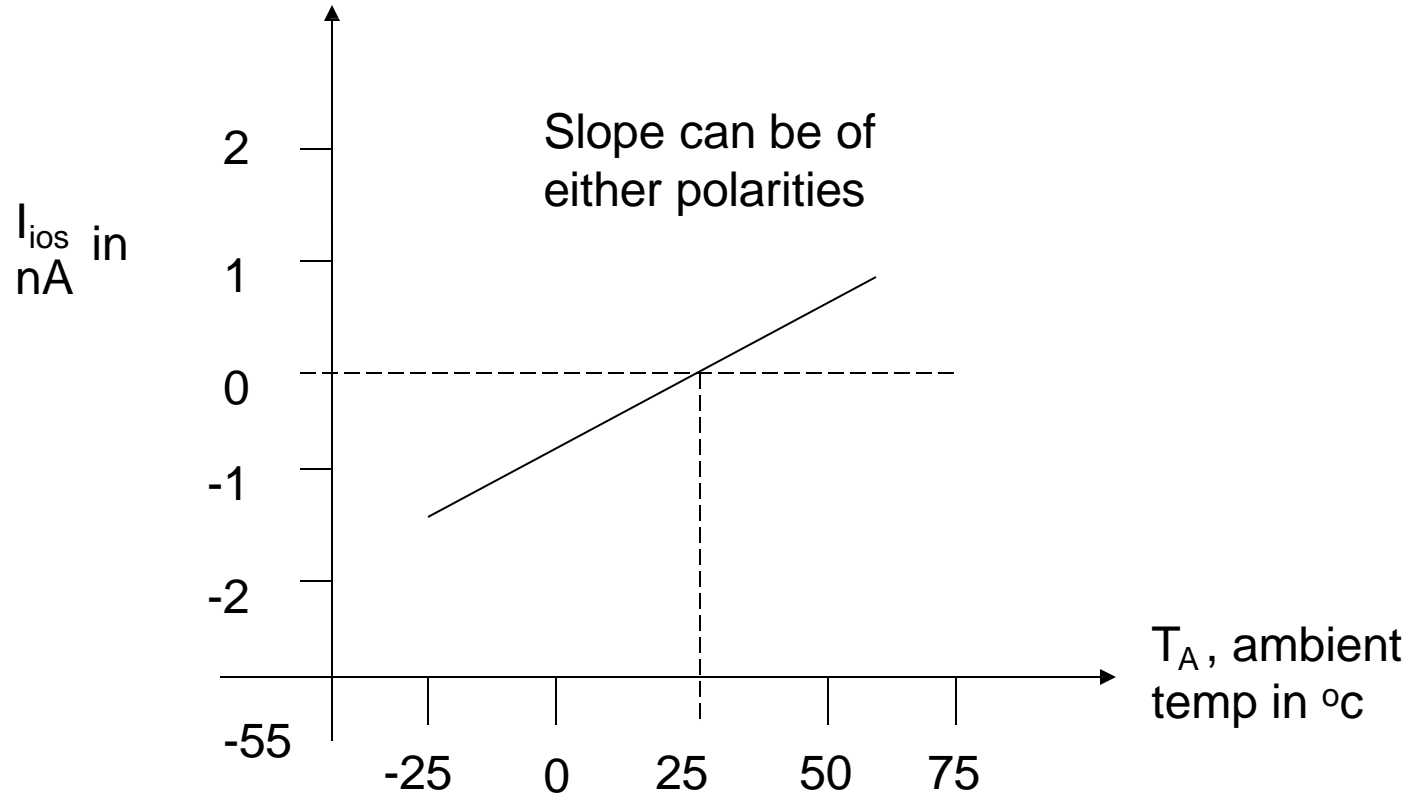
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## Input Offset current Drift



# AC Characteristics

## Frequency Response

Ideally, an op-amp should have an infinite bandwidth but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called as roll off.

The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called ***frequency response*** of the op-amp

When the gain in decibels, phase angle in degrees are plotted against logarithmic scale of frequency, the plot is called ***Bode Plot***

The manner in which the gain of the op-amp changes with variation in frequency is known as the *magnitude plot*.

The manner in which the phase shift changes with variation in frequency is known as the *phase-angle plot*.

# Obtaining the frequency response

To obtain the frequency response , consider the high frequency model of the op-amp with capacitor C at the output, taking into account the **capacitive effect** present

$$A_{OL}(f) = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

$$A_{OL}(f) = \frac{A_{OL}}{1 + j\left(\frac{f}{f_o}\right)}$$

Where

$A_{OL}(f)$  = open loop voltage gain as a function of frequency

$A_{OL}$  = Gain of the op-amp at 0Hz  
 $F$  = operating frequency

$F_o$  = Break frequency or cutoff frequency of op-amp

For a given op-amp and selected value of C, the frequency  $f_0$  is constant.

The above equation can be written in the polar form as

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_0}\right)^2}}$$

$$\angle A_{OL}(f) = \Phi(f) = -\tan^{-1}\left(\frac{f}{f_0}\right)$$

# Frequency Response of an op-amp

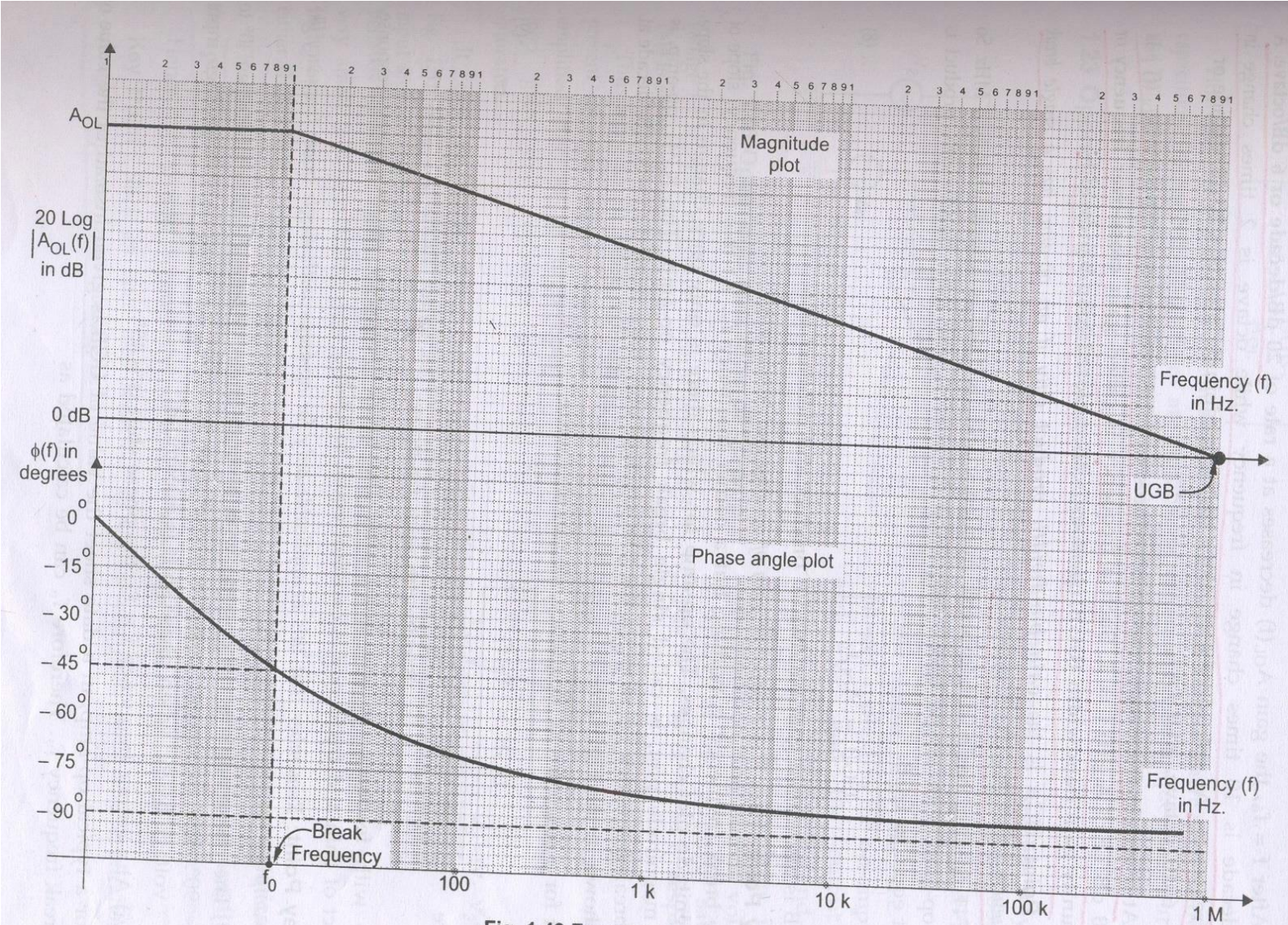


Fig. 1.49 Frequency response of an op-amp

The following observations can be made from the frequency response of an op-amp

- i) The open loop gain  $A_{OL}$  is almost constant from 0 Hz to the break frequency  $f_o$ .
- ii) At  $f=f_o$ , the gain is 3dB down from its value at 0Hz. Hence the frequency  $f_o$  is also called as -3dB frequency. It is also known as corner frequency
- iii) After  $f=f_o$ , the gain  $A_{OL}(f)$  decreases at a rate of 20 dB/decade or 6dB/octave. As the gain decreases, slope of the magnitude plot is -20dB/decade or -6dB/octave, after  $f=f_o$ .
- iv) At a certain frequency, the gain reduces to 0dB. This means  $20\log|A_{OL}|$  is 0dB i.e.  $|A_{OL}| = 1$ . Such a frequency is called gain cross-over frequency or unity gain bandwidth (UGB). It is also called closed loop bandwidth.

UGB is the gain bandwidth product only if an op-amp has a single breakover frequency, before  $A_{OL}(f)$  dB is zero.

For an op-amp with single break frequency  $f_o$  , after  $f_o$  the gain bandwidth product is constant equal to UGB

$$\text{UGB} = A_{OL} f_o$$

UGB is also called gain bandwidth product and denoted as  $f_t$  Thus  $f_t$  is the product of gain of op-amp and bandwidth.

The break frequency is nothing but a corner frequency  $f_o$  . At this frequency, slope of the magnitude plot changes. The op-amp for which there is only once change in the slope of the magnitude plot, is called single break frequency op-amp.



For a single break frequency we can also write

$$\mathbf{UGB = A_f f_f}$$

$$A_f = \text{closed loop voltage gain } F_f =$$

bandwidth with feedback

v) The phase angle of an op-amp with single break frequency varies between  $0^\circ$  to  $90^\circ$  . The maximum possible phase shift is  $-90^\circ$  , i.e. output voltage lags input voltage by  $90^\circ$  when phase shift is maximum

vi) shift is  $-45^\circ$ .

$$F_o = \mathbf{UGB / A_{oL}}$$

At a corner frequency  $f=f_o$  , the phase

Frequency $f$ in Hz	$ A_{OL}(f) $ in dB = $20 \log \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_o}\right)^2}}$ in dB	$\phi(f) = -\tan^{-1}\left(\frac{f}{f_o}\right)$ in degrees
0	106.02 dB	$0^\circ$
5	103.01 dB	$-45^\circ$
10	99.03 dB	$-63.43^\circ$
100	79.98 dB	$-87.13^\circ$
1000	60.00 dB	$-89.71^\circ$
$100 \times 10^3$	20.00 dB	$-89.99^\circ$
$1 \times 10^6$	0 dB	$-89.999^\circ$

Table 1.6

# The modes of using an op-amp

- **Open Loop** : (The output assumes one of the two possible output states, that is  $+V_{\text{sat}}$  or  $-V_{\text{sat}}$  and the amplifier acts as a switch only).
- **Closed Loop**: ( The utility of an op-amp can be greatly increased by providing negative feed back. The output in this case is not driven into saturation and the circuit behaves in a linear manner).

# Open loop configuration of op-amp

- The voltage transfer curve indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode
- Such an open loop behaviour of the op-amp finds some rare applications like voltage comparator, zero crossing detector etc.

# Open loop op-amp configurations

- The configuration in which output depends on input, but output has no effect on the input is called open loop configuration.
- No feed back from output to input is used in such configuration.
- The opamp works as high gain amplifier
- The op-amp can be used in three modes in open loop configuration they are
  1. Differential amplifier
  2. Inverting amplifier
  3. Non inverting amplifier

# Differential Amplifier

The amplifier which amplifies the difference between the two input voltages is called differential amplifier.

$$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2) = A_{OL} (V_{in1} - V_{in2})$$

Key point: For very small  $V_d$ , output gets driven into saturation due to high  $A_{OL}$ , hence this application is applicable for very small range of differential input voltage.

# Inverting Amplifier

The amplifier in which the output is inverted i.e. having 180° phase shift with respect to the input is called an inverting amplifier

$$V_o = -A_{OL} V_{in2}$$

Keypoint: The negative sign indicates that there is phase shift of 180° between input and output i.e. output is inverted with respect to input.

# Non-inverting Amplifier

The amplifier in which the output is amplified without any phase shift in between input and output is called non inverting amplifier

$$V_o = A_{OL} V_{in1}$$

Keypoint: The positive output shows that input and output are in phase and input is amplified  $A_{OL}$  times to get the output.



# Why op-amp is generally not used in open loop mode?

As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level. Thus in open loop configuration, the output is at its positive saturation voltage ( $+V_{\text{sat}}$ ) or negative saturation voltage ( $-V_{\text{sat}}$ ) depending on which input  $V_1$  or  $V_2$  is more than the other. For a.c. input voltages, output may switch between positive and negative saturation voltages

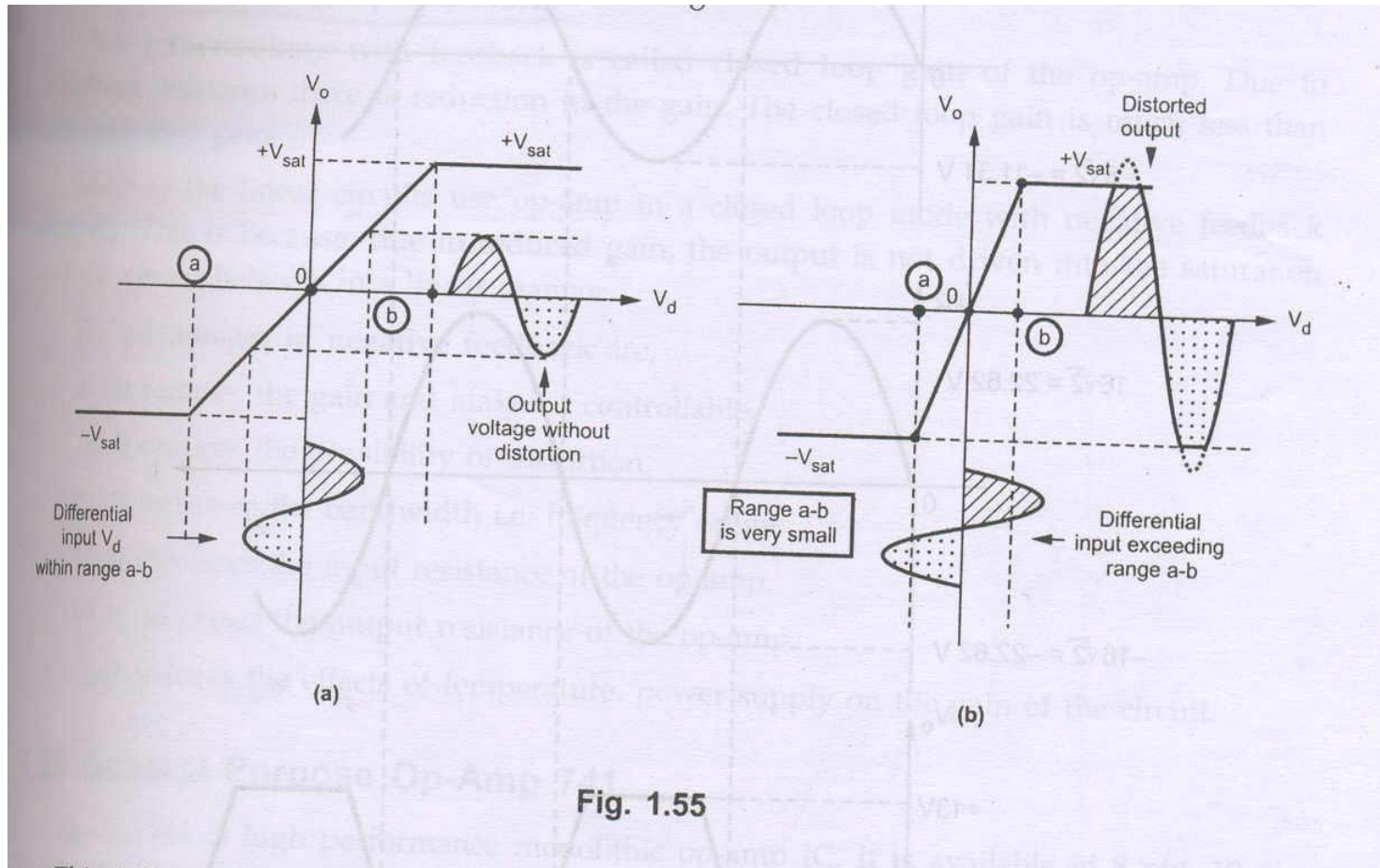


Fig. 1.55

This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode. Hence the op-amp in open loop configuration is not used for the linear applications

# General purpose op-amp 741

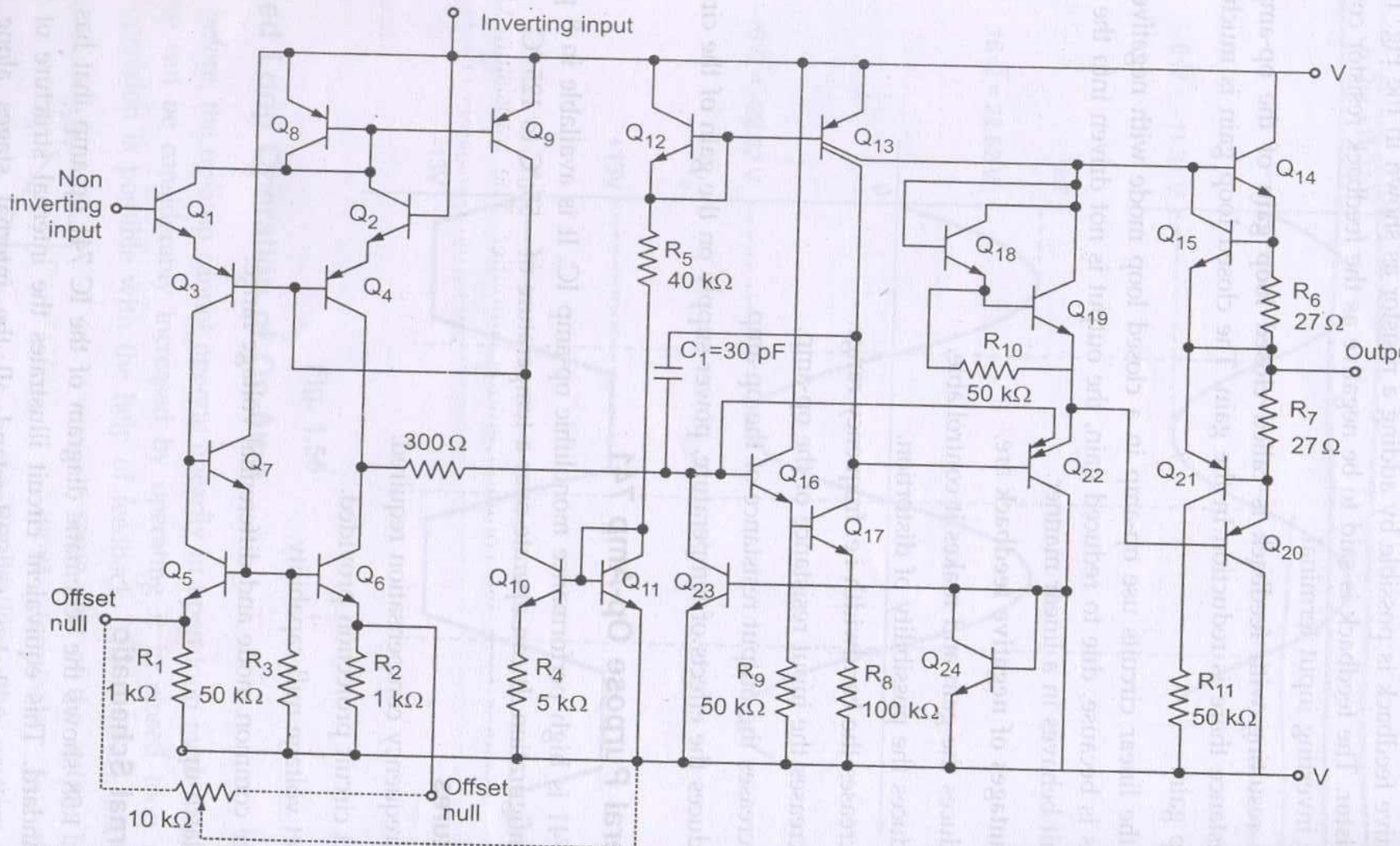
The IC 741 is high performance monolithic op-amp IC. It is available in 8pin, 10pin or 14pin configuration. It can operate over a temperature of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## Features:

- i) No frequency compensation required
- ii) Short circuit protection provided
- iii) Offset Voltage null capability
- iv) Large common mode and differential voltage range
- v) No latch up

# Internal schematic of 741 op-amp

Fig. 1.58 Internal schematic of IC 741



# The 8pin DIP package of IC 741

The 8 pin DIP package of IC 741 is shown in the Fig. 1.59.

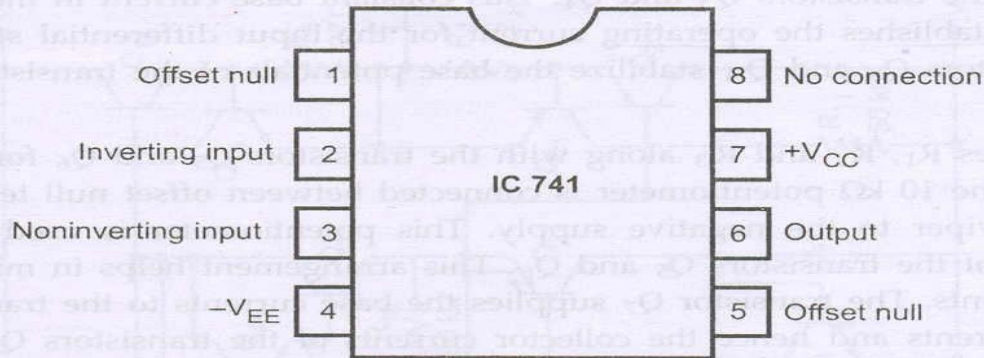


Fig. 1.59 8 Pin diagram

## 1.26.3 Ideal Vs Practical Characteristics of IC 741 Op-Amp

The Table 1.7 lists the ideal op-amp characteristics and the typical characteristics of 741 IC, a popular general purpose op-amp IC.

Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	$A_{OL}$	$\infty$	$2 \times 10^5$
2	Output impedance	$Z_{out}$	0	$75 \Omega$
3	Input impedance	$Z_{in}$	$\infty$	$2 M\Omega$
4	Input offset current	$I_{ios}$	0	20 nA
5	Input offset voltage	$V_{ios}$	0	1 mV
6	Bandwidth	B.W	$\infty$	1 MHz
7	CMRR	$\rho$	$\infty$	90 dB
8	Slew rate	S	$\infty$	$0.5 V/\mu\text{sec}$
9	Input bias current	$I_b$	0	80 nA
10	PSRR	PSRR	0	$30 \mu V/V$

Table 1.7

## Realistic simplifying assumptions

- **Zero input current:** The current drawn by either of the input terminals (inverting and non-inverting) is zero
- **Virtual ground :** This means the differential input voltage  $V_d$  between the non-inverting and inverting terminals is essentially zero. (The voltage at the non inverting input terminal of an op-amp can be realistically assumed to be equal to the voltage at the inverting input terminal)

## Closed loop operation of op-amp

The utility of the op-amp can be increased considerably by operating in closed loop mode. The closed loop operation is possible with the help of feedback. The feedback allows to feed some part of the output back to the input terminals. In the linear applications, the op-amp is always used with negative feedback. The negative feedback helps in controlling gain, which otherwise drives the op-amp out of its linear range, even for a small noise voltage at the input terminals

# Ideal Inverting Amplifier

1. The output is inverted with respect to input, which is indicated by minus sign.
2. The voltage gain is independent of open loop gain of the op-amp, which is assumed to be large.
3. The voltage gain depends on the ratio of the two resistances.

Hence selecting  $R_f$  and  $R_1$ , the required value of gain can be easily obtained.

4. If  $R_f > R_1$ , the gain is greater than 1 If  $R_f < R_1$ , the gain is less than 1

If  $R_f = R_1$ , the gain is unity

Thus the output voltage can be greater than, less than or equal to the input voltage in magnitude



5. If the ratio of  $R_f$  and  $R_1$  is  $K$  which is other than one, the circuit is called **scale changer** while for  $R_f/R_1 = 1$  it is called **phase inverter**.
6. The closed loop gain is denoted as  $A_{VF}$  or  $A_{CL}$  i.e. gain with feedback

# Ideal Non-inverting Amplifier

1. The voltage gain is always greater than one
2. The voltage gain is positive indicating that for a.c. input, the output and input are in phase while for d.c. input, the output polarity is same as that of input
3. The voltage gain is independent of open loop gain of op-amp, but depends only on the two resistance values
4. The desired voltage gain can be obtained by selecting proper values of  $R_f$  and  $R_1$

# Comparison of the ideal inverting and non-inverting op-amp

Ideal Inverting amplifier	Ideal non-inverting amplifier
1. Voltage gain= $-R_f/R_1$	1. Voltage gain= $1+R_f/R_1$
2. The output is inverted with respect to input	2. No phase shift between input and output
3. The voltage gain can be adjusted as greater than, equal to or less than one	3. The voltage gain is always greater than one
4. The input impedance is $R_1$	4. The input impedance is very large

# Practical Inverting Amplifier

Closed Loop Voltage gain =

$$A_{CL} = - \frac{A_{OL} R_f}{R_1 + R_f + R_1 A_{OL}}$$

# Practical Non-Inverting Amplifier

Closed Loop Voltage gain =

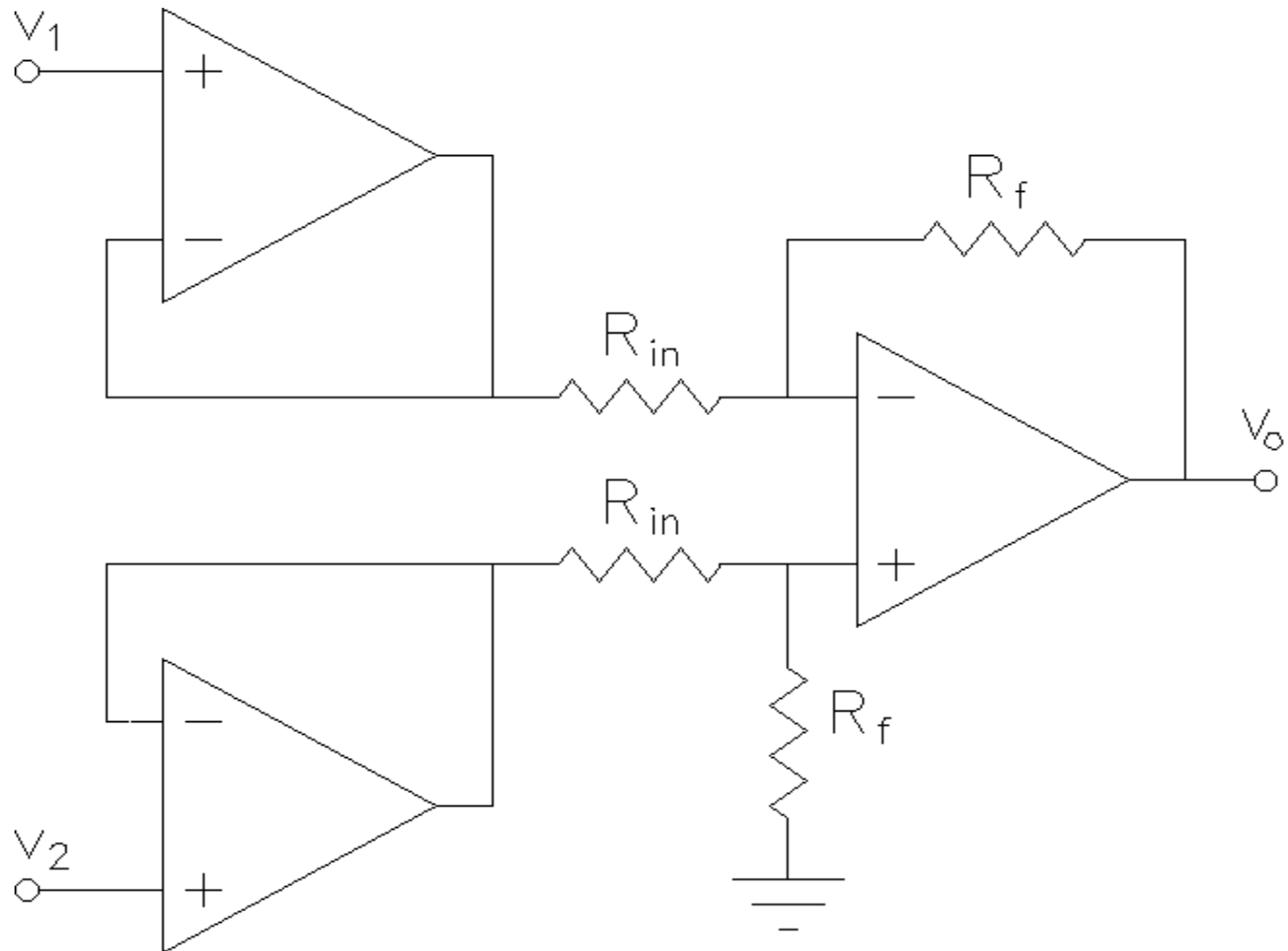
$$A_{CL} = \frac{A_{OL} (R_1 + R_f)}{R_1 + R_f + R_1 A_{OL}}$$



# Instrumentation Amplifier

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

# Instrumentation Amplifier



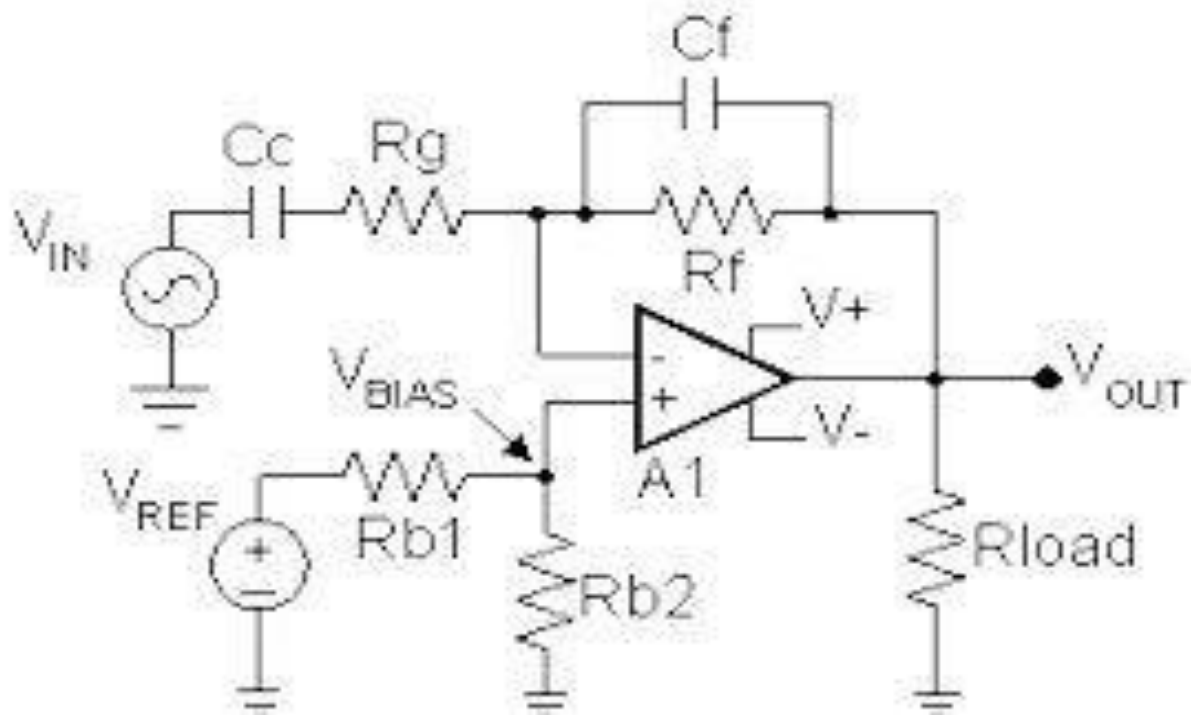


# Features of instrumentation amplifier

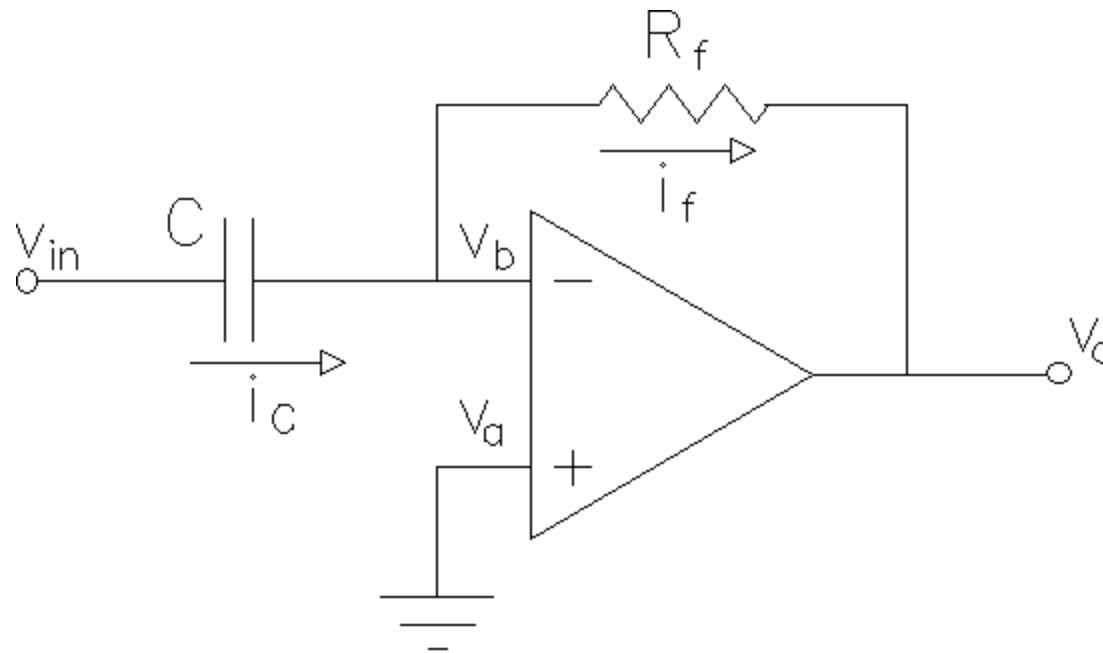
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature coefficient
4. low dc offset
5. low output impedance



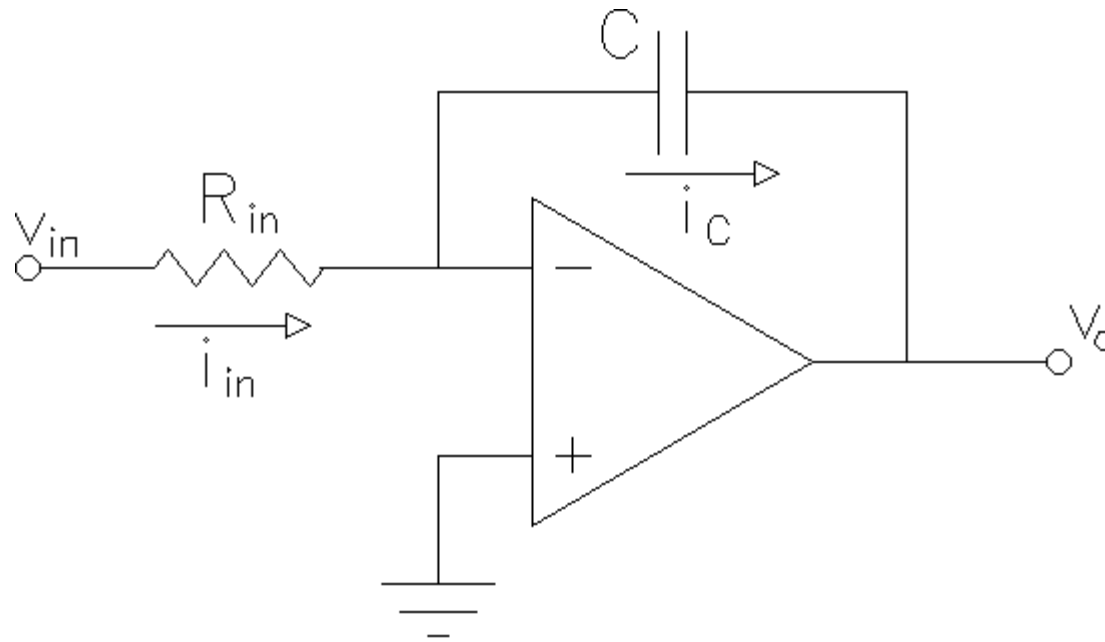
# AC AMPLIFIER



# Differentiator



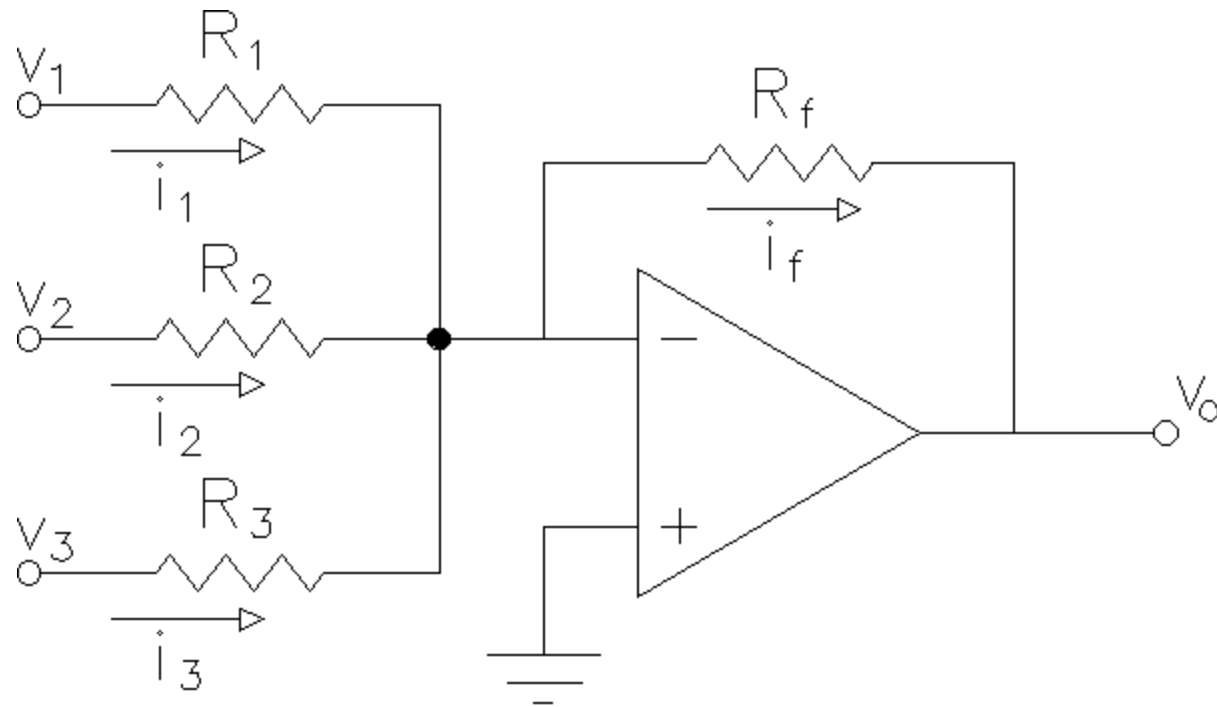
# Integrator



# Differential amplifier

This circuit amplifies only the difference between the two inputs. In this circuit there are two resistors labeled  $R_{IN}$  Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

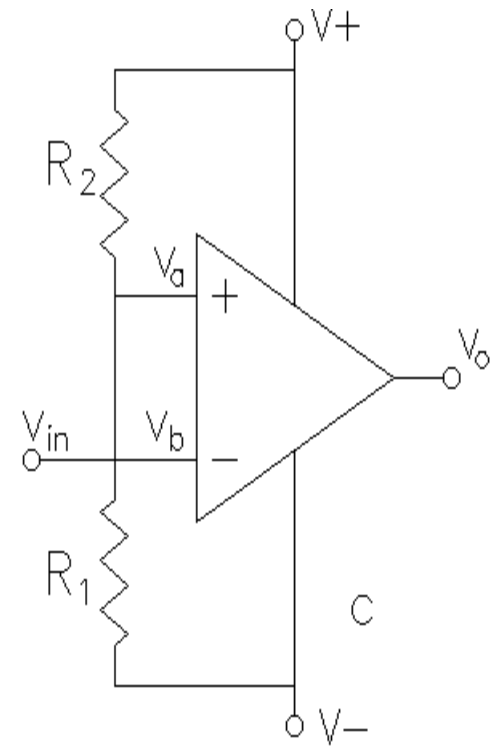
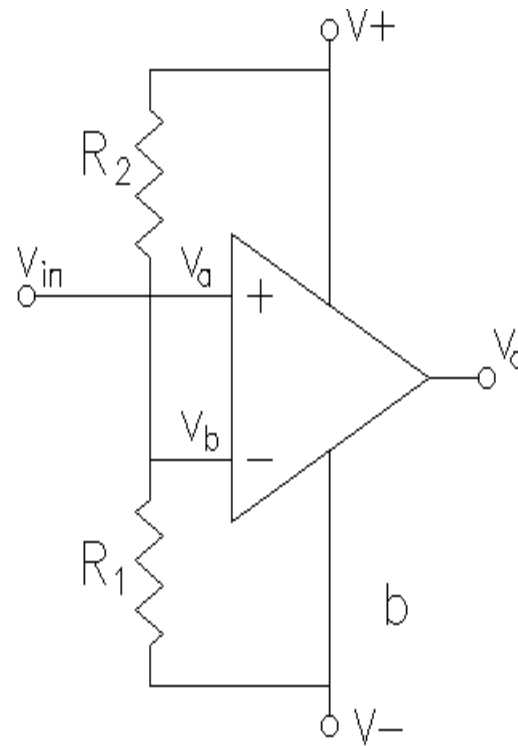
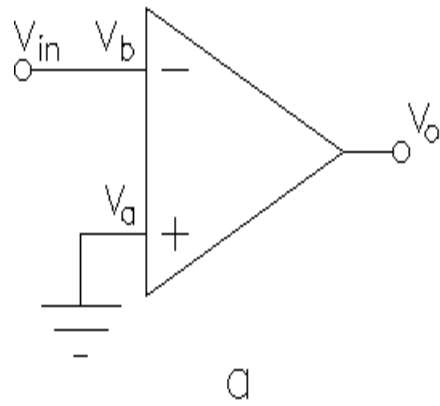
# Summer



# Comparator

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output +  $V_{sat}$

# Comparator



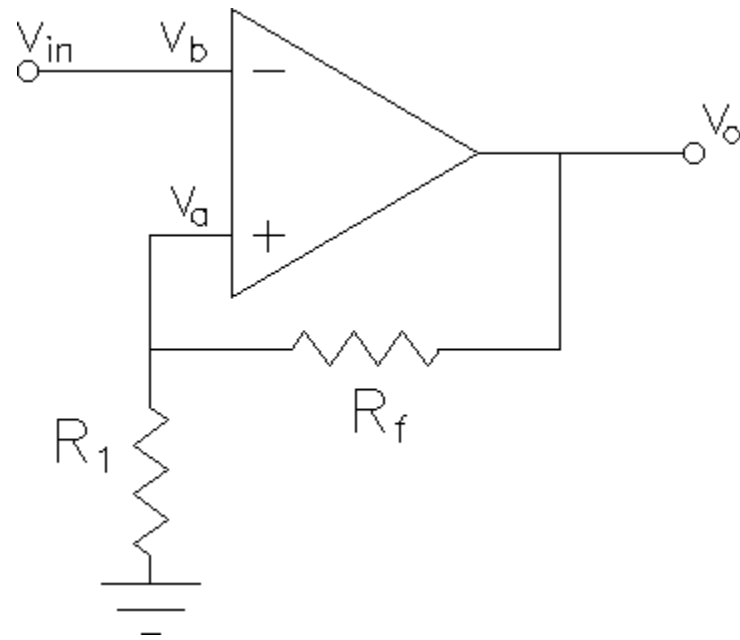



# Applications of comparator

1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector



# Schmitt trigger





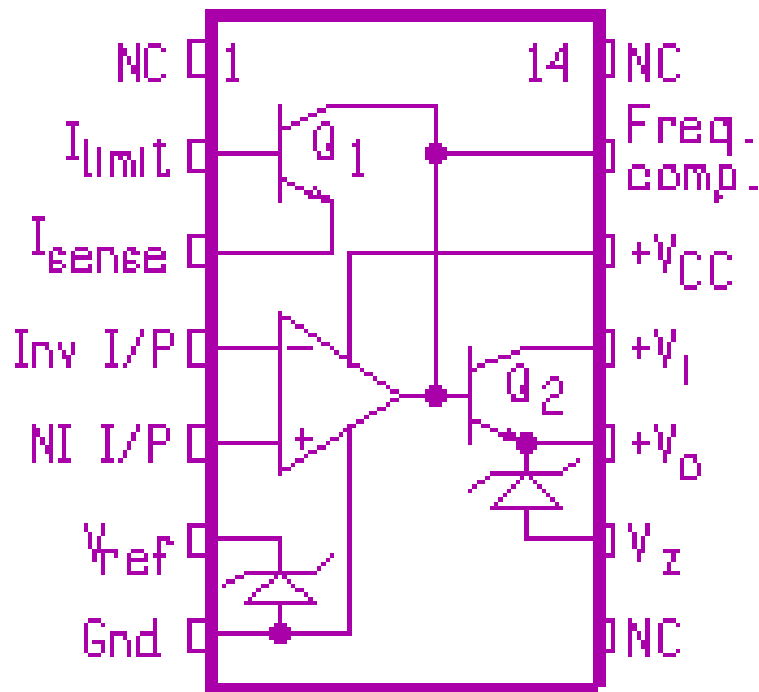
# INTRODUCTION TO VOLTAGE REGULATORS

- A **voltage regulator** is designed to automatically maintain a constant **voltage** level. A **voltage regulator** may be a simple "feed-forward" design or may include negative feedback control loops. It may use an electromechanical mechanism, or electronic components.

# IC Voltage Regulators

- There are basically two kinds of IC voltage regulators:
  - Multipin type, e.g. LM723C
  - 3-pin type, e.g. 78/79XX
- Multipin regulators are less popular but they provide the greatest flexibility and produce the highest quality voltage regulation
- 3-pin types make regulator circuit design simple

# Multipin IC Voltage Regulator



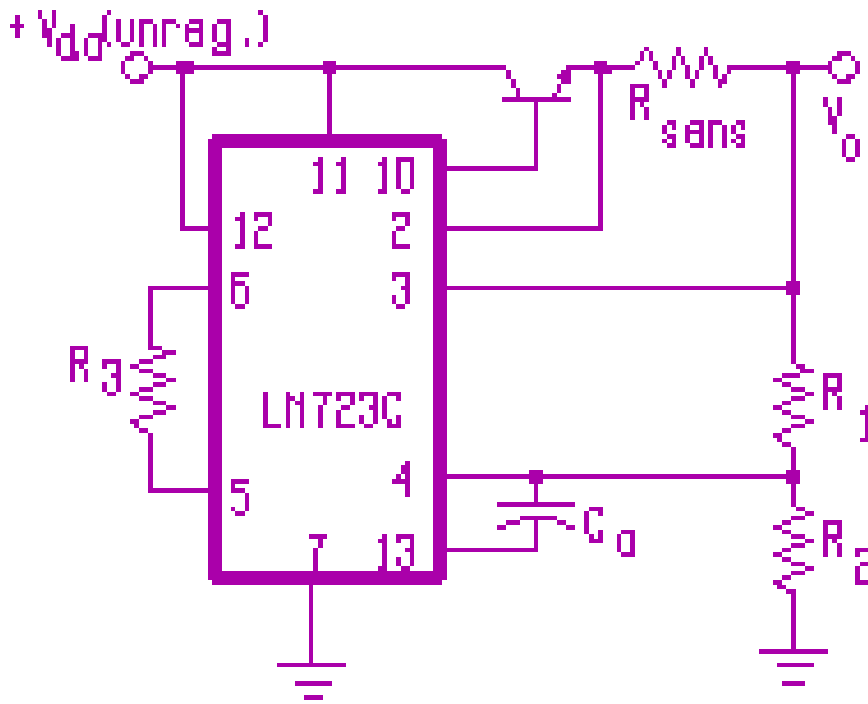
- The LM723 has an equivalent circuit that contains most of the parts of the op-amp voltage regulator discussed earlier.
- It has an internal voltage reference, error amplifier, pass transistor, and current limiter all in one IC package.

LM 723C Schematic

# LM723 Voltage Regulator

- Can be either 14-pin DIP or 10-pin TO-100 can
- May be used for either +ve or -ve, variable or fixed regulated voltage output
- Using the internal reference (7.15 V), it can operate as a high-voltage regulator with output from 7.15 V to about 37 V, or as a low-voltage regulator from 2 V to 7.15 V
- Max. output current with heat sink is 150 mA
- Dropout voltage is 3 V (i.e.  $V_{CC} > V_{o(max)} + 3$ )

# LM723 in High-Voltage Configuration



External pass transistor and current sensing added.

Design equations:

$$V_o = \frac{V_{ref} (R_1 + R_2)}{R_2}$$

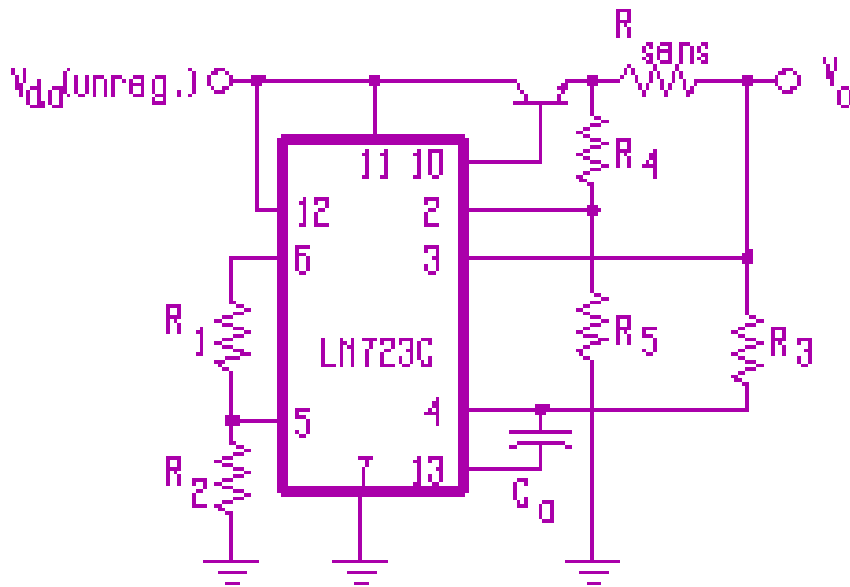
$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \quad R_{sens} = \frac{0.7}{I_{max}}$$

Choose  $R_1 + R_2 = 10$  k $\Omega$ ,

and  $C_c = 100$  pF.

To make  $V_o$  variable, replace  $R_1$  with a pot.

# LM723 in Low-Voltage Configuration



With external pass transistor  
and foldback current limiting

$$V_o = \frac{R_2 V_{ref}}{R_1 + R_2}$$

$$I_{L(max)} = \frac{R_4 V_o + 0.7(R_4 + R_5)}{R_5 R_{sens}}$$

$$I_{short} = \frac{0.7(R_4 + R_5)}{R_5 R_{sens}}$$

$$R_{sens} = \frac{0.7V_o}{I_{short}(V_o + 0.7) - 0.7I_{L(max)}}$$

Under foldback condition:

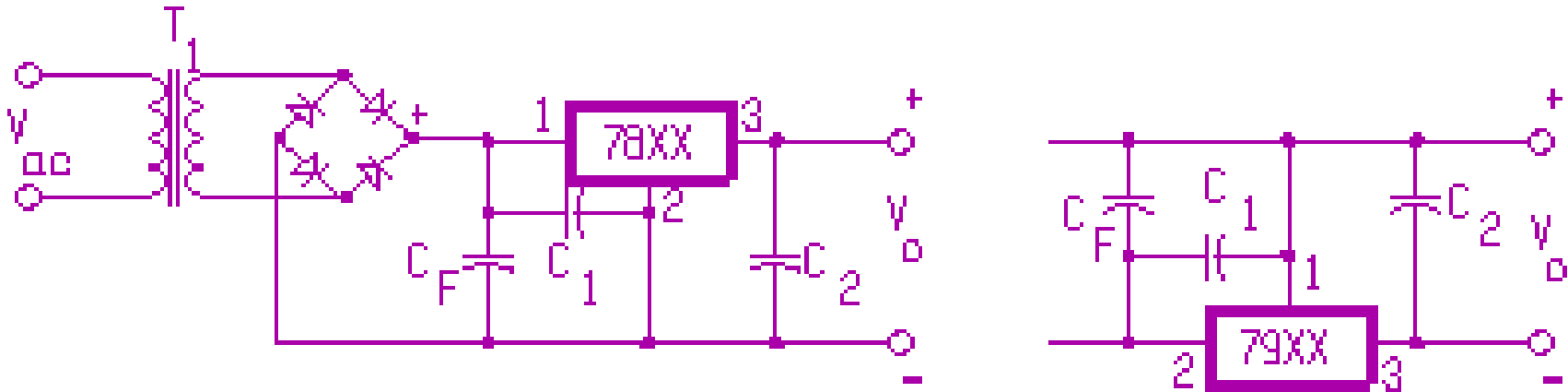
$$V_o' = \frac{0.7R_L(R_4 + R_5)}{R_5 R_{sens} - R_4 R_L}$$

# Three-Terminal Fixed Voltage Regulators

- Less flexible, but simple to use
- Come in standard TO-3 (20 W) or TO-220 (15 W) transistor packages
- 78/79XX series regulators are commonly available with 5, 6, 8, 12, 15, 18, or 24 V output
- Max. output current with heat sink is 1 A
- Built-in thermal shutdown protection
- 3-V dropout voltage; max. input of 37 V
- Regulators with lower dropout, higher in/output, and better regulation are available.

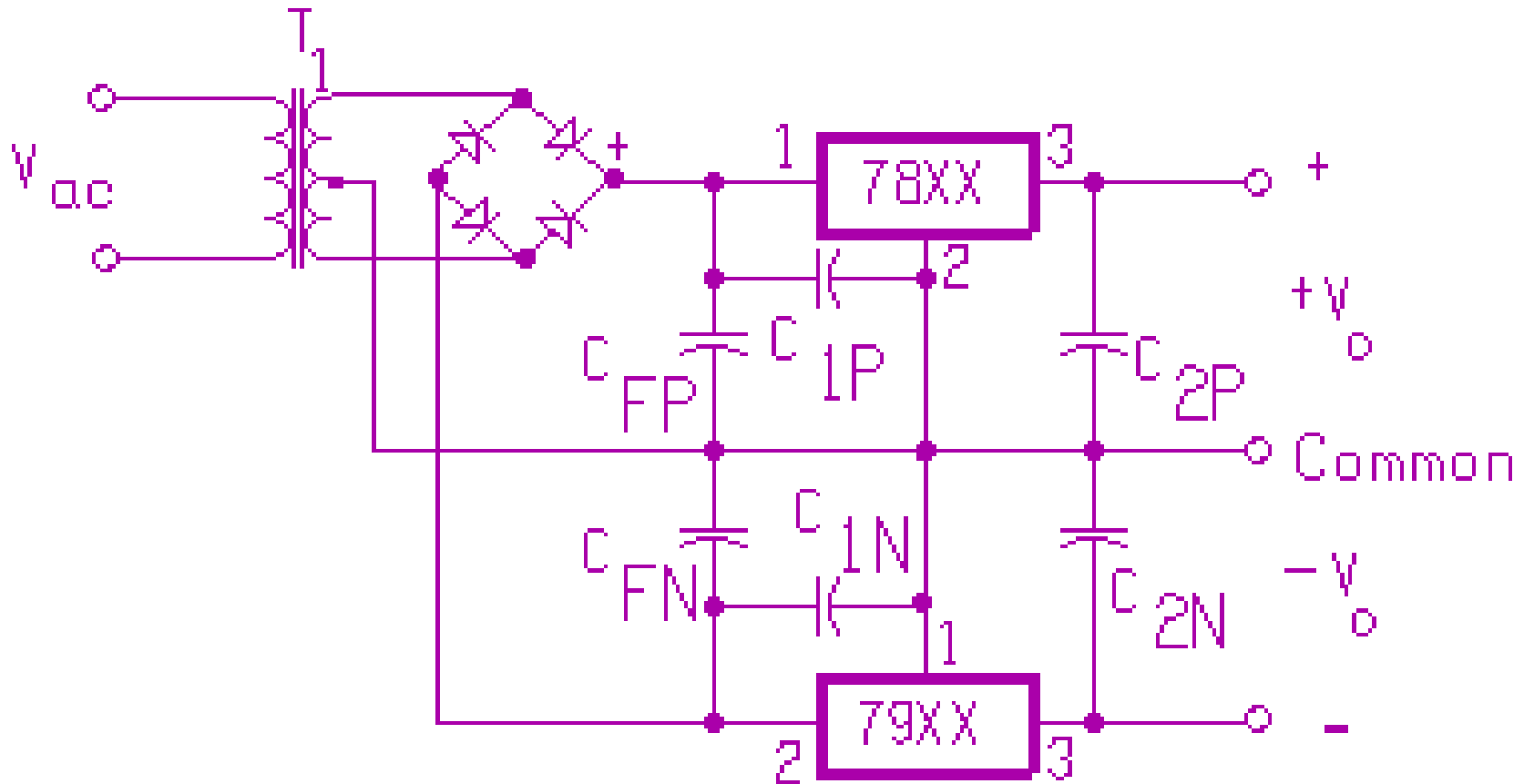


# Basic Circuits With 78/79XX Regulators

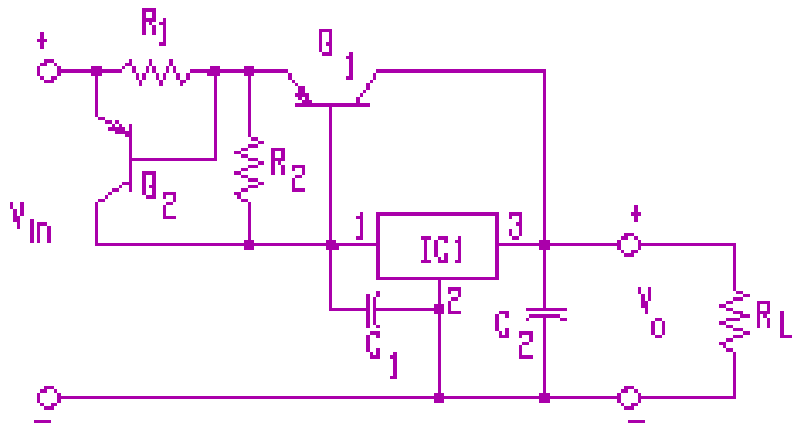


- Both the 78XX and 79XX regulators can be used to provide +ve or -ve output voltages
- $C_1$  and  $C_2$  are generally optional.  $C_1$  is used to cancel any inductance present, and  $C_2$  improves the transient response. If used, they should preferably be either  $1 \mu\text{F}$  tantalum type or  $0.1 \mu\text{F}$  mica type capacitors.

# Dual-Polarity Output with 78/79XX Regulators



# 78XX Regulator with Pass Transistor

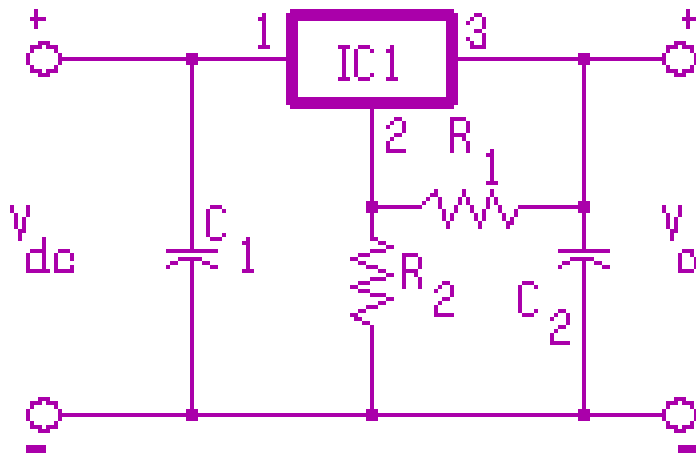


$$R_1 = \frac{0.7}{I_{max}}$$

$$R_2 = \frac{0.7}{I_{R2}}$$

- $Q_1$  starts to conduct when  $V_{R2} = 0.7 \text{ V}$ .
- $R_2$  is typically chosen so that max.  $I_{R2}$  is 0.1 A.
- Power dissipation of  $Q_1$  is  $P = (V_i - V_o)I_L$ .
- $Q_2$  is for current limiting protection. It conducts when  $V_{R1} = 0.7 \text{ V}$ .
- $Q_2$  must be able to pass max. 1 A; but note that max.  $V_{CE2}$  is only 1.4 V.

# 78XX Floating Regulator



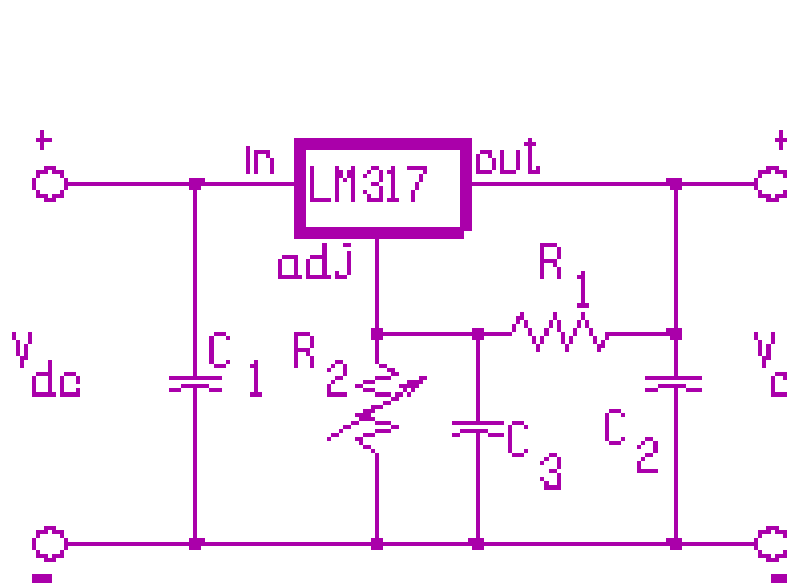
- It is used to obtain an output  $>$  the  $V_{reg}$  value up to a max. of 37 V.
- $R_1$  is chosen so that  $R_1 \approx 0.1 V_{reg}/I_Q$ , where  $I$  is the

$$V_o = V_{reg} + \left( \frac{V_{reg}}{R_1} + I_Q \right) R_2$$

## 3-Terminal Variable Regulator

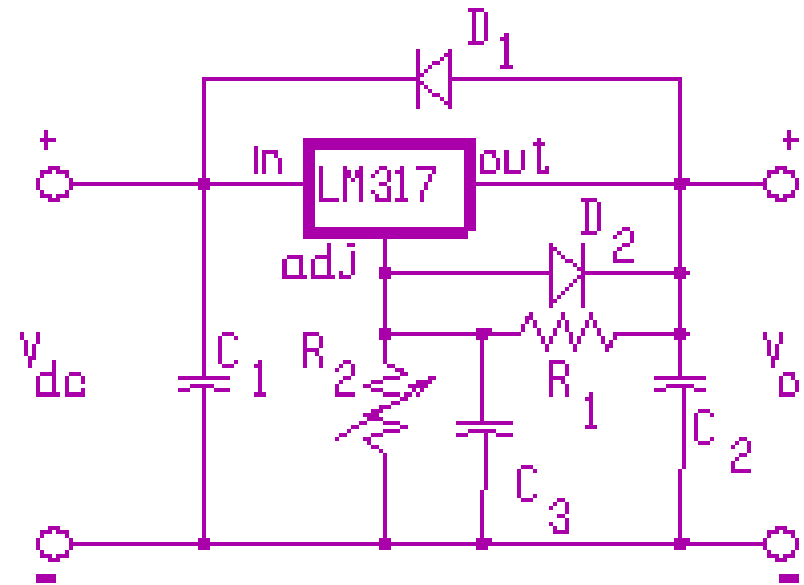
- The floating regulator could be made into a variable regulator by replacing  $R_2$  with a pot. However, there are several disadvantages:
  - Minimum output voltage is  $V_{reg}$  instead of 0 V.
  - $I_Q$  is relatively large and varies from chip to chip.
  - Power dissipation in  $R_2$  can in some cases be quite large resulting in bulky and expensive equipment.
- A variety of 3-terminal variable regulators are available, e.g. LM317 (for +ve output) or LM 337 (for -ve output).

# Basic LM317 Variable Regulator Circuits



(a)

Circuit with capacitors to improve performance



(b)

Circuit with protective diodes

# Notes on Basic LM317 Circuits

- The function of  $C_1$  and  $C_2$  is similar to those used in the 78/79XX fixed regulators.
- $C_3$  is used to improve ripple rejection.
- Protective diodes in circuit (b) are required for high-current/high-voltage applications.

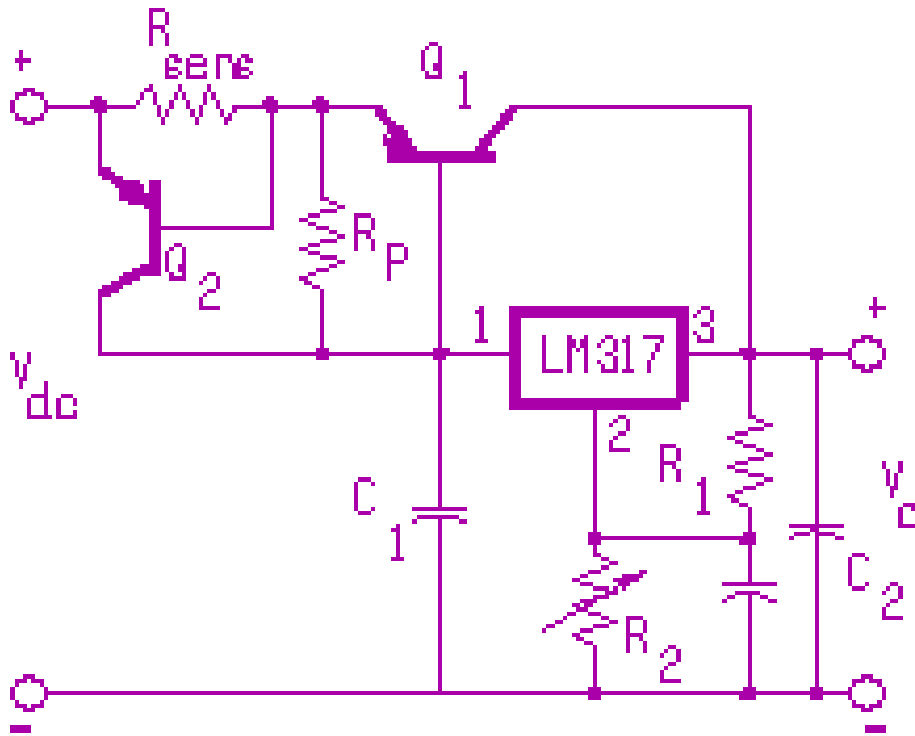
$$V_o = V_{ref} + \left( \frac{V_{ref}}{R_1} + I_{adj} \right) R_2$$

$$R_2 = \frac{R_1 (V_o - V_{ref})}{V_{ref} + I_{adj} R_1}$$

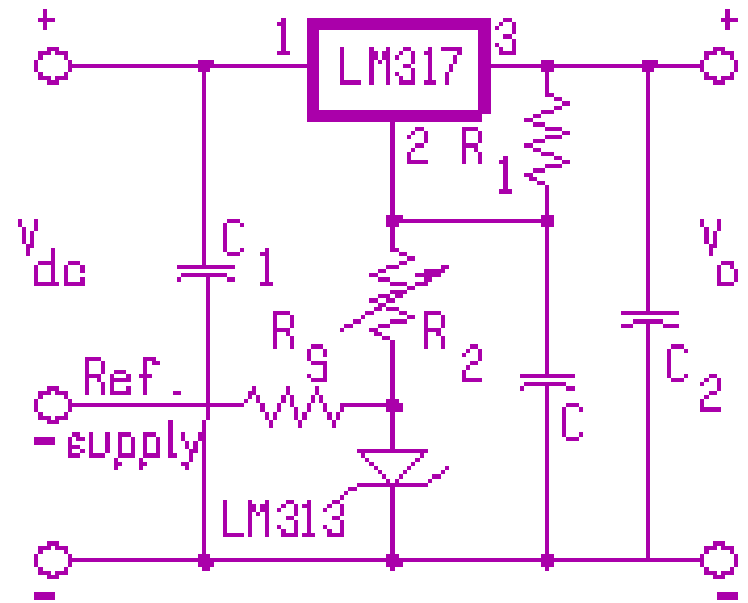
where  $V_{ref} = 1.25$  V, and  $I_{adj}$  is the current flowing into the adj. terminal (typically  $50 \mu\text{A}$ ).

$R_1 = V_{ref} / I_{L(\min)}$ , where  $I_{L(\min)}$  is typically  $10$  mA.

# LM317 Regulator Circuits



Circuit with pass transistor and current limiting



Circuit to give 0V min. output voltage



# UNIT –II

- Opamp -555
- IC-565 applications

# Filter

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

## Type of Filter

1. Passive filters
2. Active filters

# Passive filters

Passive filters work well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive. For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

# Active filters

Active filters used op-amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop, inductor less active filters can be obtained

# some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter
5. All pass filter

# Active Filters

- Active filters use op-amp(s) and RC components.
- Advantages over passive filters:
  - op-amp(s) provide gain and overcome circuit losses
  - increase input impedance to minimize circuit loading
  - higher output power
  - sharp cutoff characteristics can be produced simply and efficiently without bulky inductors
- Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

# Review of Filter Types & Responses

- 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop
- 0 dB attenuation in the passband (usually)
- 3 dB attenuation at the *critical* or *cutoff frequency*,  $f_c$  (for Butterworth filter)
- Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements).  
Attenuation at any frequency  $f$  is:

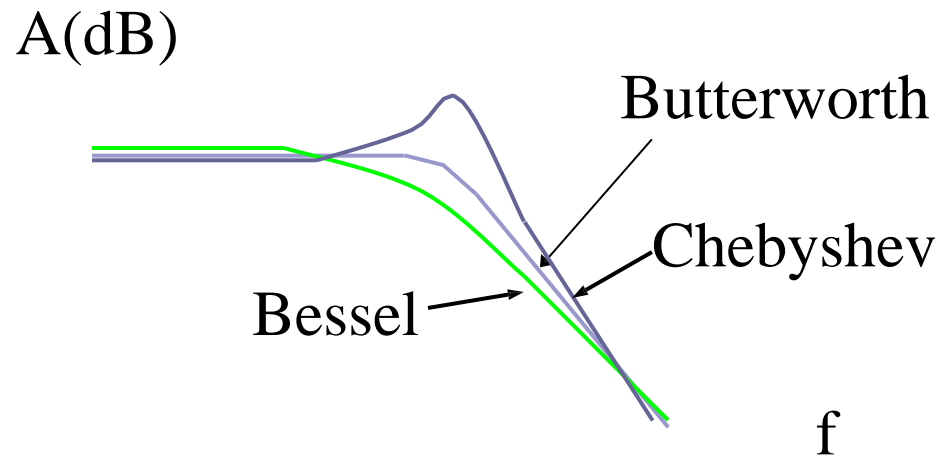
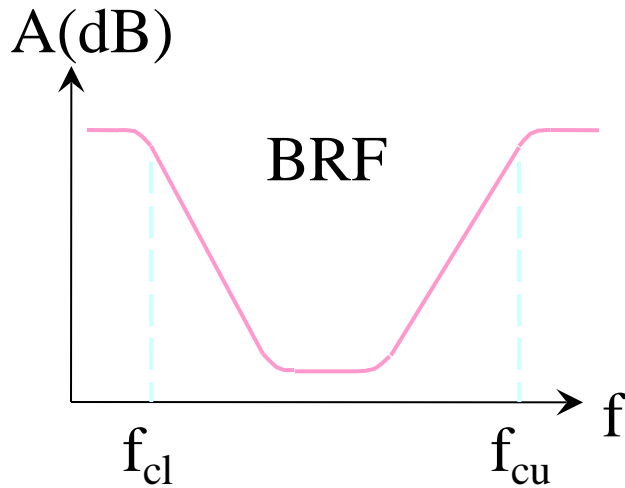
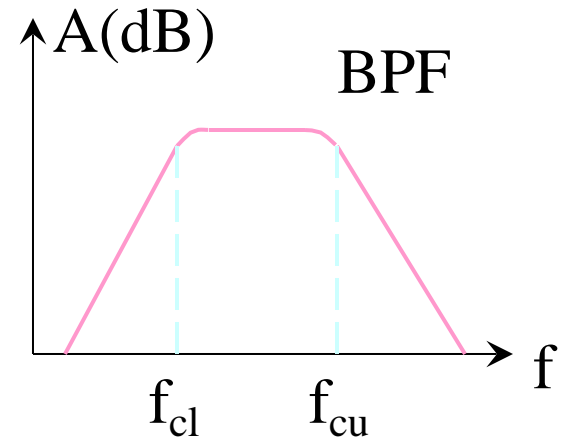
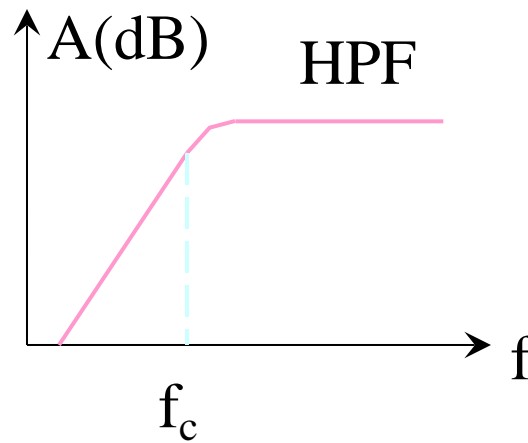
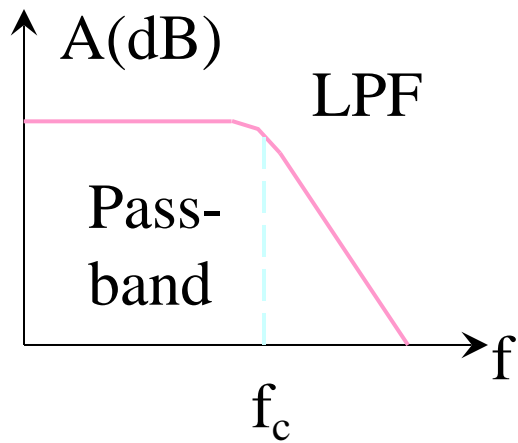
$$\text{atten. (dB) at } f = \log\left(\frac{f}{f_c}\right) \times \text{atten. (dB) at } f_{dec}$$

# Review of Filters (cont'd)

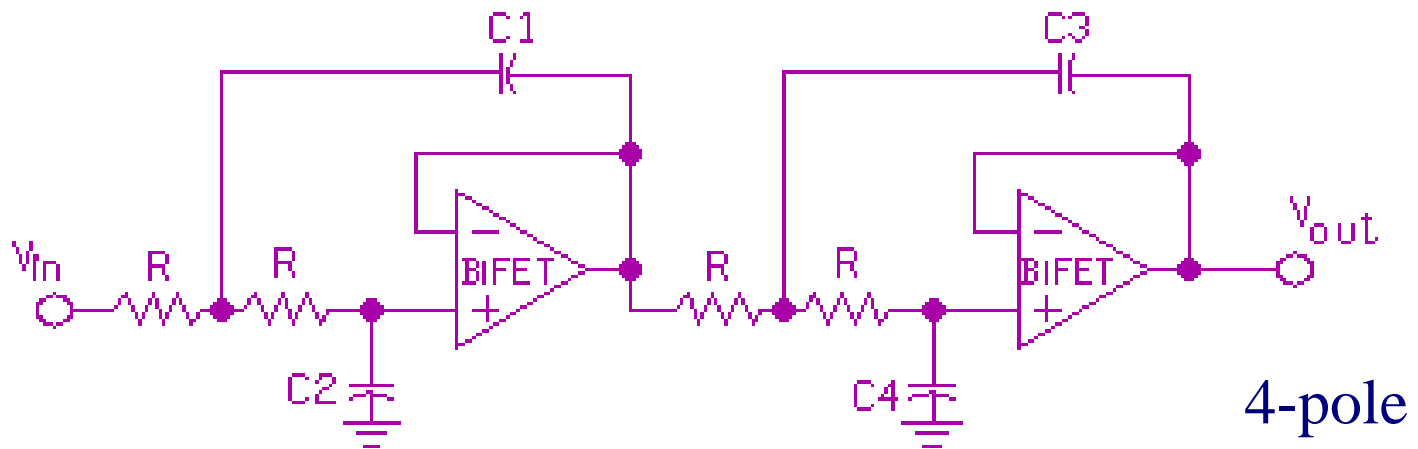
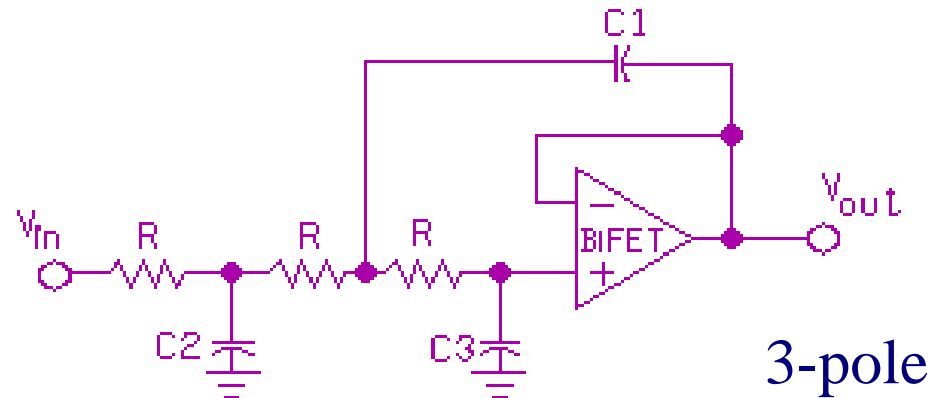
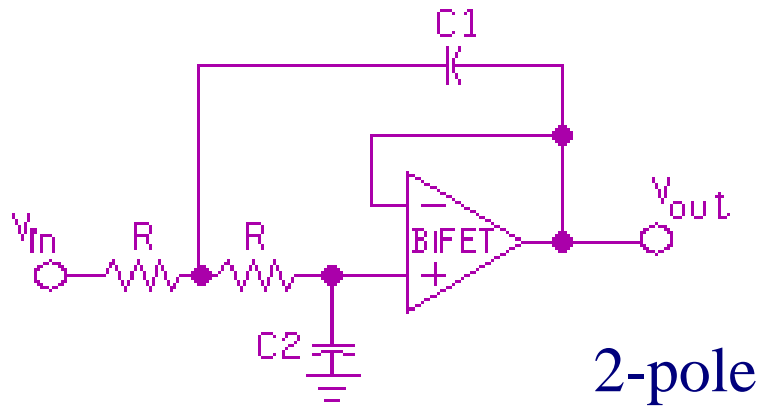
- Bandwidth of a filter:  $BW = f_{cu} - f_{cl}$
- Phase shift:  $45^\circ/\text{pole}$  at  $f_c$ ;  $90^\circ/\text{pole}$  at  $\gg f_c$
- 4 types of filter responses are commonly used:
  - Butterworth - maximally flat in passband; highly non-linear phase response with frequency
  - Bessel - gentle roll-off; linear phase shift with frequency
  - Chebyshev - steep initial roll-off with ripples in passband
  - Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stopband



# Frequency Response of Filters



# Unity-Gain Low-Pass Filter Circuits



# Design Procedure for Unity-Gain LPF

- ★ Determine/select number of poles required.
- 📖 Calculate the frequency scaling constant,  $K_f = 2\pi f$
- ✳️ Divide normalized C values (from table) by  $K_f$  to obtain frequency-scaled C values.
- ✳️ Select a desired value for one of the frequency-scaled C values and calculate the impedance scaling factor:

$$K_x = \frac{\text{frequency - scaled } C \text{ value}}{\text{desired } C \text{ value}}$$

- ⊞ Divide all frequency-scaled C values by  $K_x$
- ⊕ Set  $R = K_x \Omega$

## An Example

Design a unity-gain LP Butterworth filter with a critical frequency of 5 kHz and an attenuation of at least 38 dB at 15 kHz.

The attenuation at 15 kHz is 38 dB

⑧ the attenuation at 1 decade (50 kHz) = 79.64 dB.

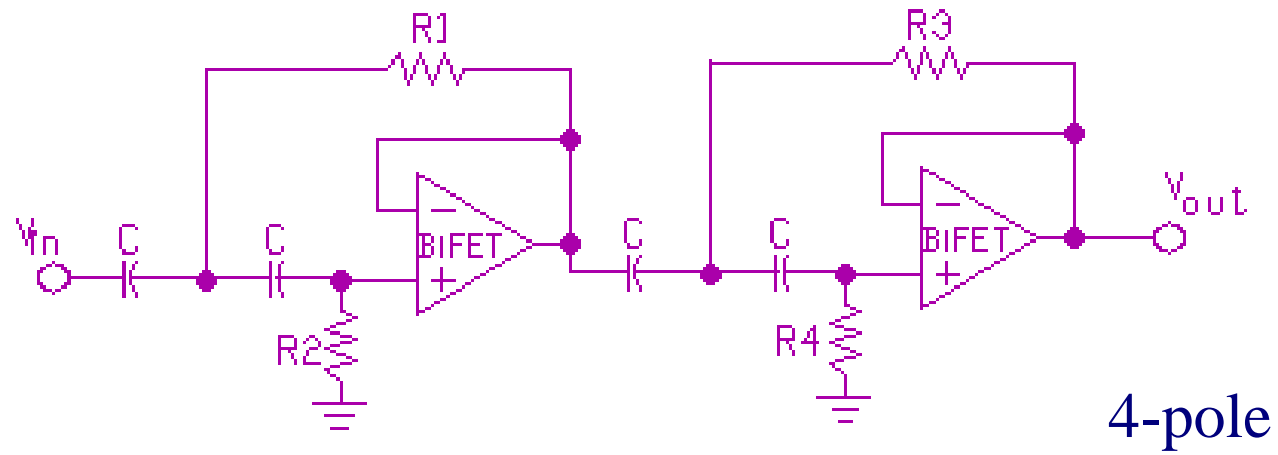
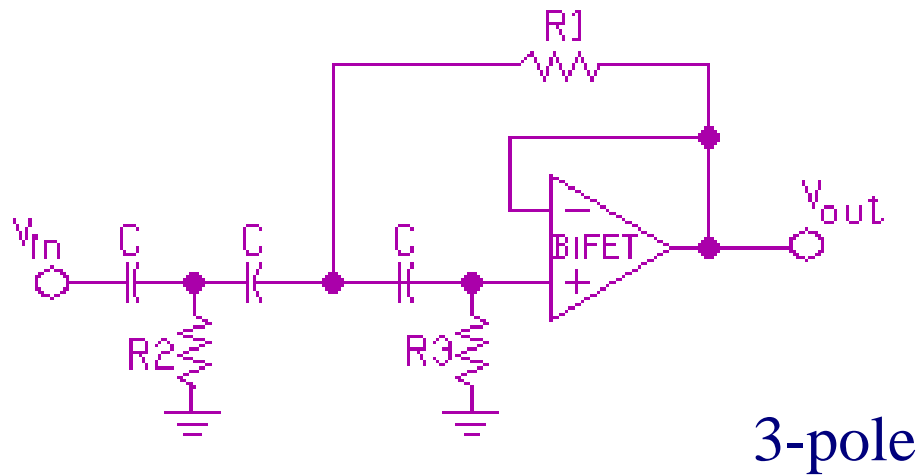
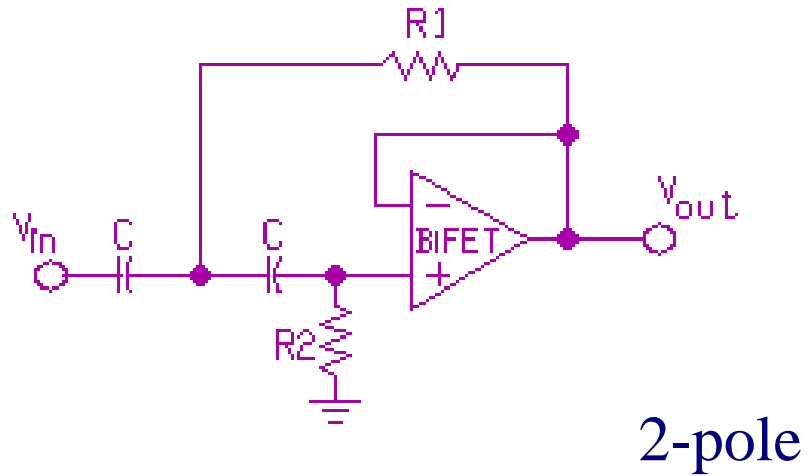
We require a filter with a roll-off of at least 4 poles.

$K_f = 31,416$  rad/s. Let's pick  $C_1 = 0.01 \mu\text{F}$  (or 10 nF). Then  $C_2 = 8.54$  nF,  $C_3 = 24.15$  nF, and  $C_4 = 3.53$  nF.

Pick standard values of 8.2 nF, 22 nF, and 3.3 nF.  $K_x = 3,444$

Make all  $R = 3.6$  k $\Omega$  (standard value)

# Unity-Gain High-Pass Filter Circuits

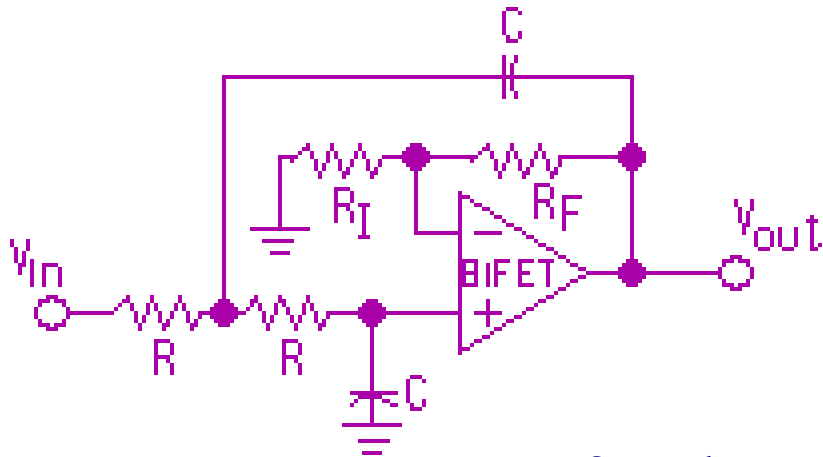


# Design Procedure for Unity-Gain HPF

- The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by  $K_f$ . Then pick a desired value for C, such as 0.001  $\mu\text{F}$  to 0.1  $\mu\text{F}$ , to calculate  $K_x$ . (Note that all capacitors have the same value).
- For step #6, multiply all normalized R values (from table) by  $K_x$ .

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.:  $C = 0.01 \mu\text{F}$ ,  $R_1 = 4.49 \text{ k}\Omega$ ,  $R_2 = 11.43 \text{ k}\Omega$ ,  $R_3 = 78.64 \text{ k}\Omega$ .; pick standard values of 4.3  $\text{k}\Omega$ , 11  $\text{k}\Omega$ , and 75  $\text{k}\Omega$ ).

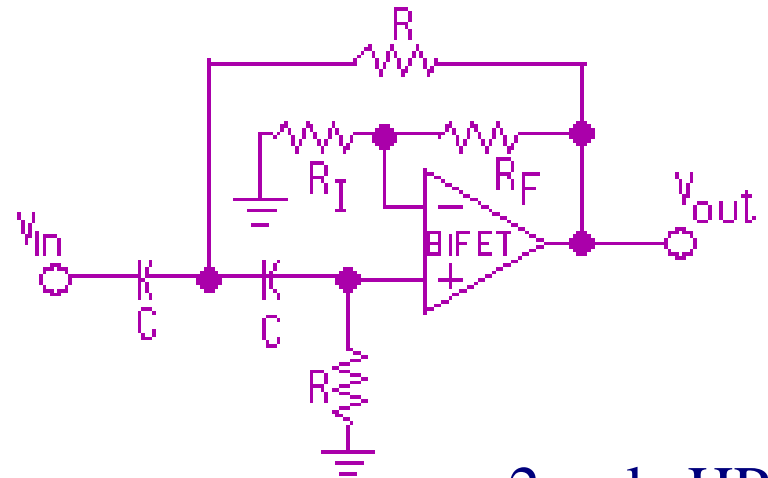
# Equal-Component Filter Design



2-pole LPF

Same value R & same value C are used in filter.

Select C (e.g. 0.01  $\mu\text{F}$ ), then:



2-pole HPF

$A_v$  for # of poles is given in a table and is the same for

LP and HP filter design.

$$A_v = \frac{R_F}{R_I} + 1$$

# Example

Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

Choose  $C = 0.01 \mu\text{F}$ ;    ⑧  $R = 5.3 \text{ k}\Omega$

From table,  $A_{v1} = 1.1523$ , and  $A_{v2} = 2.2346$ .

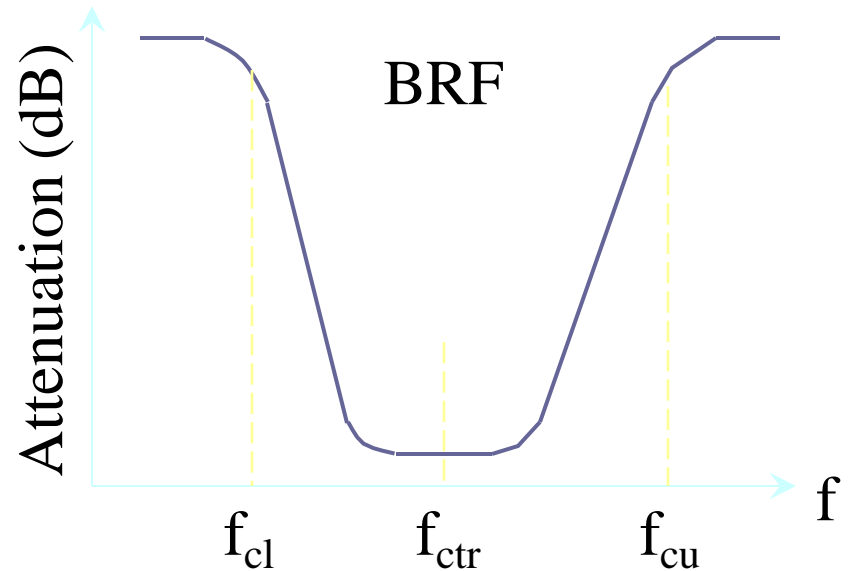
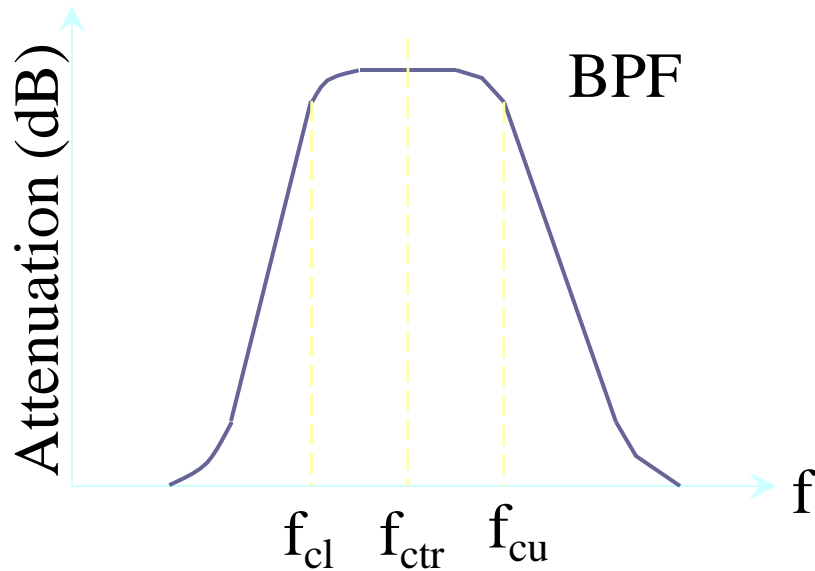
Choose  $R_{I1} = R_{I2} = 10 \text{ k}\Omega$ ; then  $R_{F1} = 1.5 \text{ k}\Omega$ , and

$R_{F2} =$   
12.3 k $\Omega$  .

Select standard values: 5.1 k $\Omega$ , 1.5 k $\Omega$ , and 12 k $\Omega$ .



# Bandpass and Band-Rejection Filter



The quality factor,  $Q$ , of a filter is given by:

where  $BW = f_{cu} - f_{cl}$  and

$$f_{ctr} = \sqrt{f_{cu} f_{cl}}$$

$$Q = \frac{f_{ctr}}{BW}$$

# More On Bandpass Filter

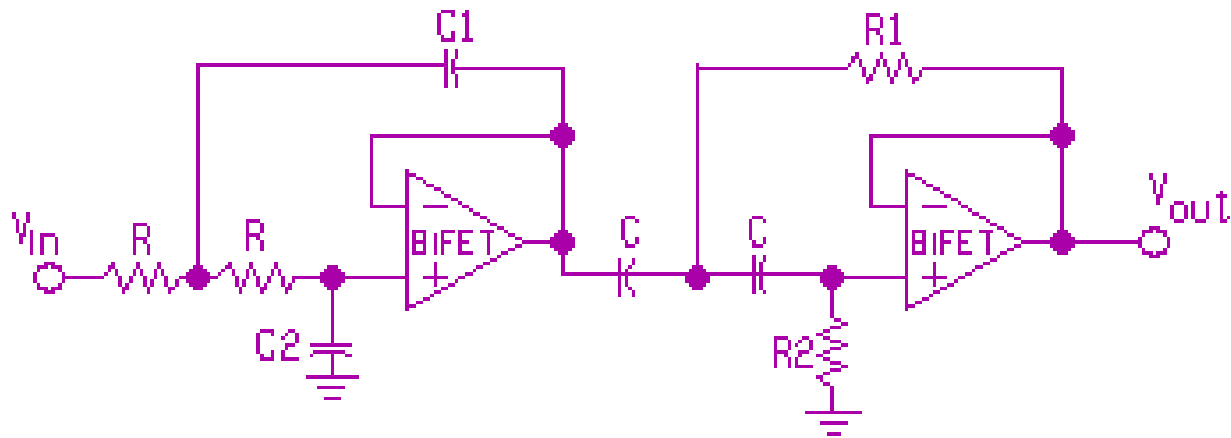
If BW and  $f_{\text{centre}}$  are given, then:

A *broadband* BPF can be obtained by combining a LPF and a HPF:

$$f_{cl} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} - \frac{BW}{2} ; f_{cu} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} + \frac{BW}{2}$$

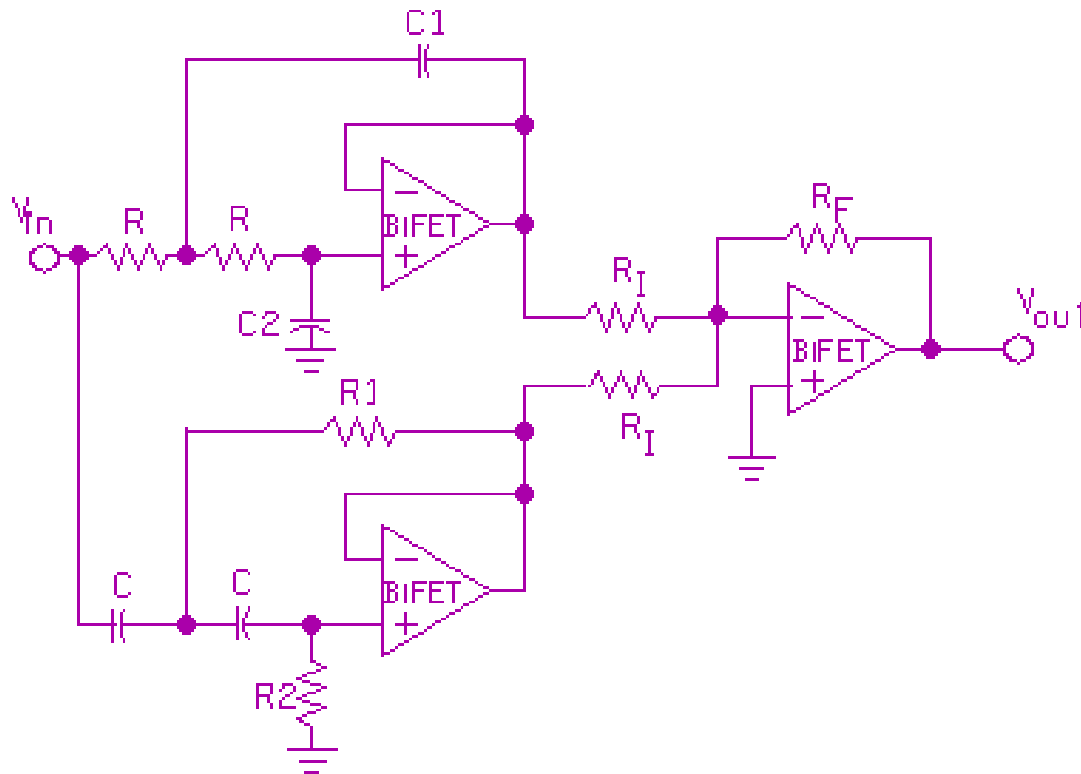
The Q of this filter is usually

> 1.



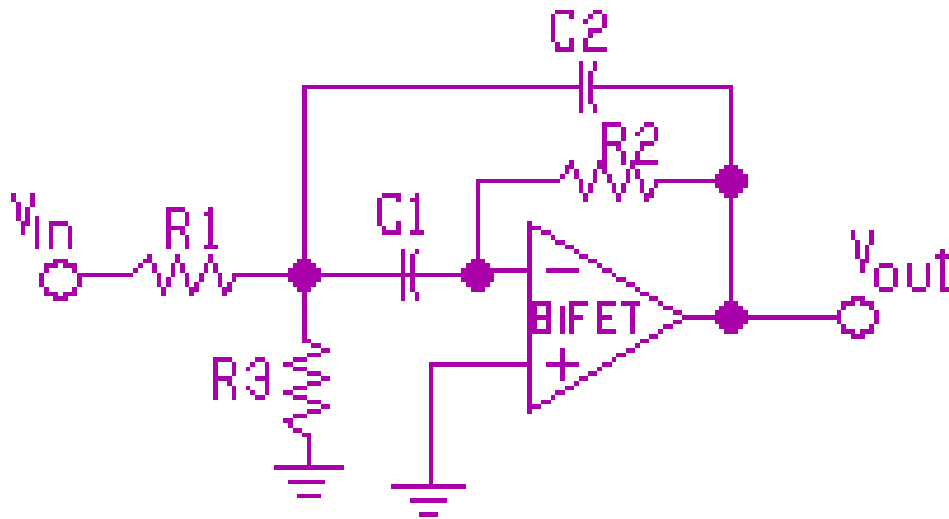
# Broadband Band-Reject Filter

A LPF and a HPF can also be combined to give a broadband BRF:



2-pole band-reject filter

# Narrow-band Bandpass Filter



$$BW = \frac{f_{ctr}}{Q} = \frac{1}{Q}$$

$$C1 = C2 = C = \frac{1}{2\pi R_1 Q}$$

$$R_2 = 2R_1$$

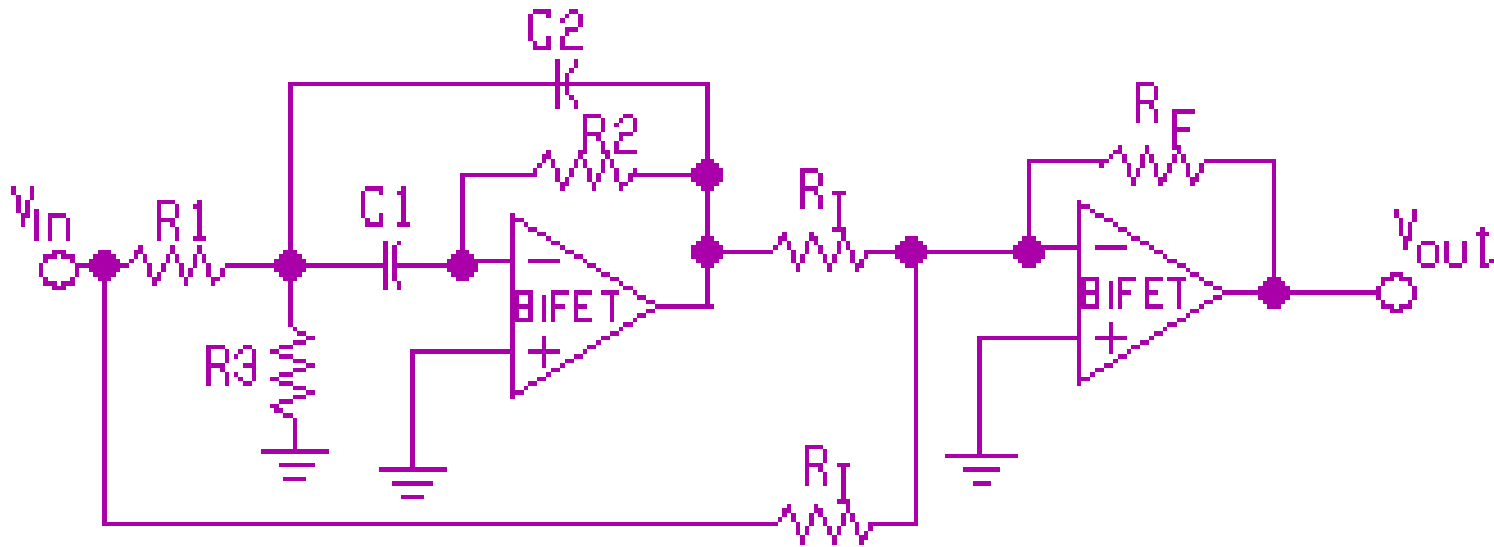
$$R_3 = \frac{R_1}{2Q^2 - 1}$$

$$f_{ctr} = \frac{1}{2\pi R_1 C} \sqrt{1 + \frac{R_1}{R_3}}$$

$R_3$  can be adjusted or trimmed to change  $f_{ctr}$  without affecting the BW. Note that  $Q < 1$ .

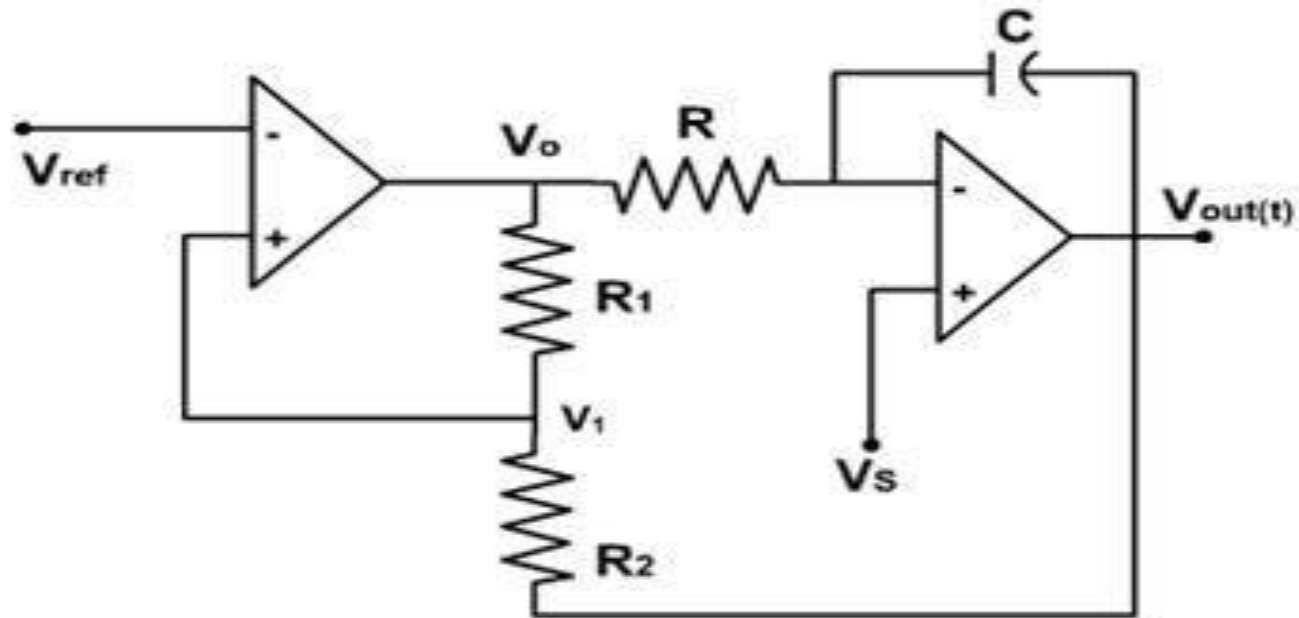
# Narrow-band Band-Reject Filter

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal:



The equations for  $R_1$ ,  $R_2$ ,  $R_3$ ,  $C_1$ , and  $C_2$  are the same as before.  $R_I = R_F$  for unity gain and is often chosen to be  $\gg R_1$ .

# TRIANGULAR WAVE GENERATOR



# 555 IC

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.

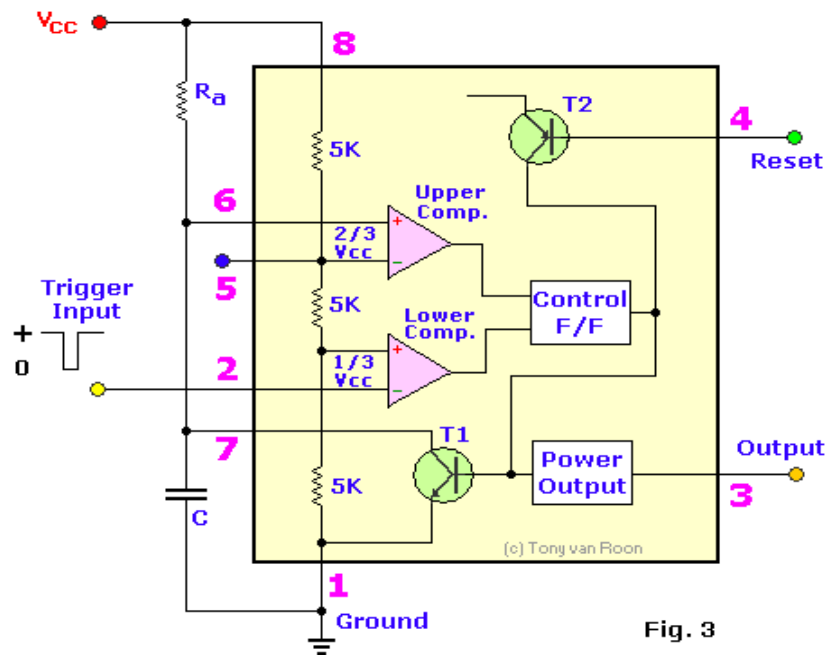


Fig. 3



# Features of 555 Timer Basic blocks

1. It has two basic operating modes: monostable and astable
2. It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
3. It has very high temperature stability

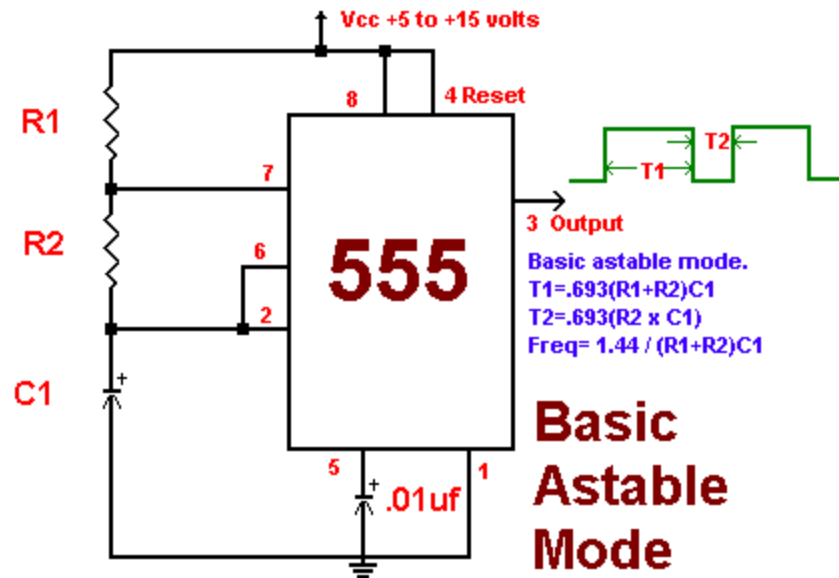




# Applications of 555 Timer

1. astable multivibrator
2. monostable multivibrator
3. Missing pulse detector
4. Linear ramp generator
5. Frequency divider
6. Pulse width modulation
7. FSK generator
8. Pulse position modulator
9. Schmitt trigger

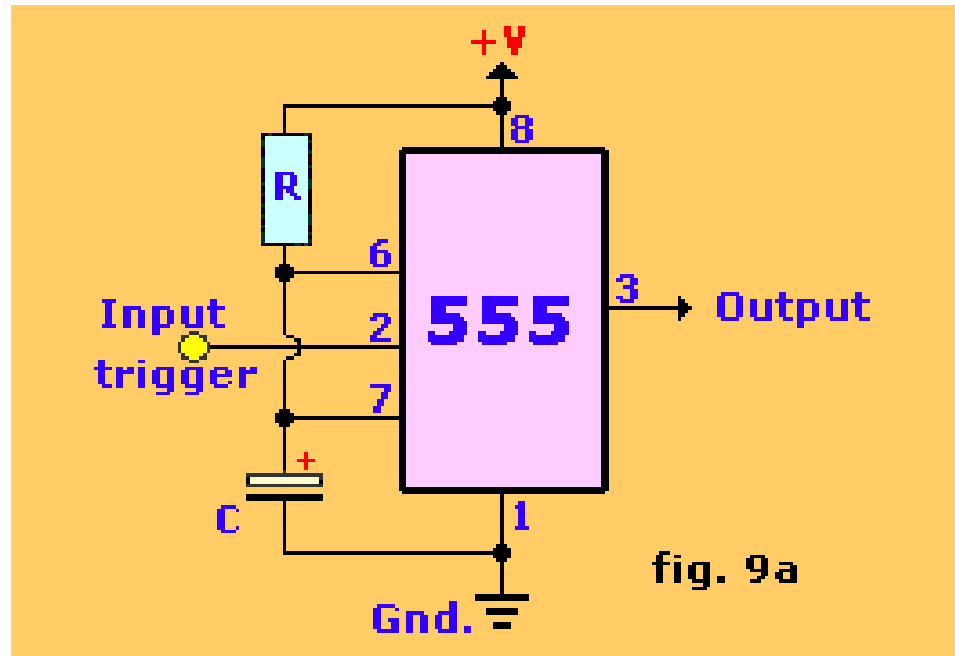
# Astable multivibrator



# Astable multivibrator

- When the voltage on the capacitor reaches  $(2/3)V_{cc}$ , a switch is closed at pin 7 and the capacitor is discharged to  $(1/3)V_{cc}$ , at which time the switch is opened and the cycle starts over

# Monostable multivibrator



# Voltage controlled oscillator

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

## The features of 566 VCO

1. Wide supply voltage range(10- 24V)
2. Very linear modulation characteristics
3. High temperature stability

# UNIT - III

- DATA  
CONVERTERS

# Classification of ADCs

1. Direct type ADC.
2. Integrating type ADC

## Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

# Integrating type converters

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter





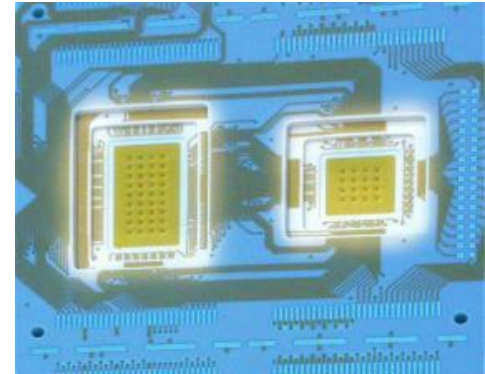
# **Digital Logic families**

# Overview

- Integration, Moore's law
- Early families (DL, RTL)
- TTL
- Evolution of TTL family
- ECL
- CMOS family and its evolution
- Overview

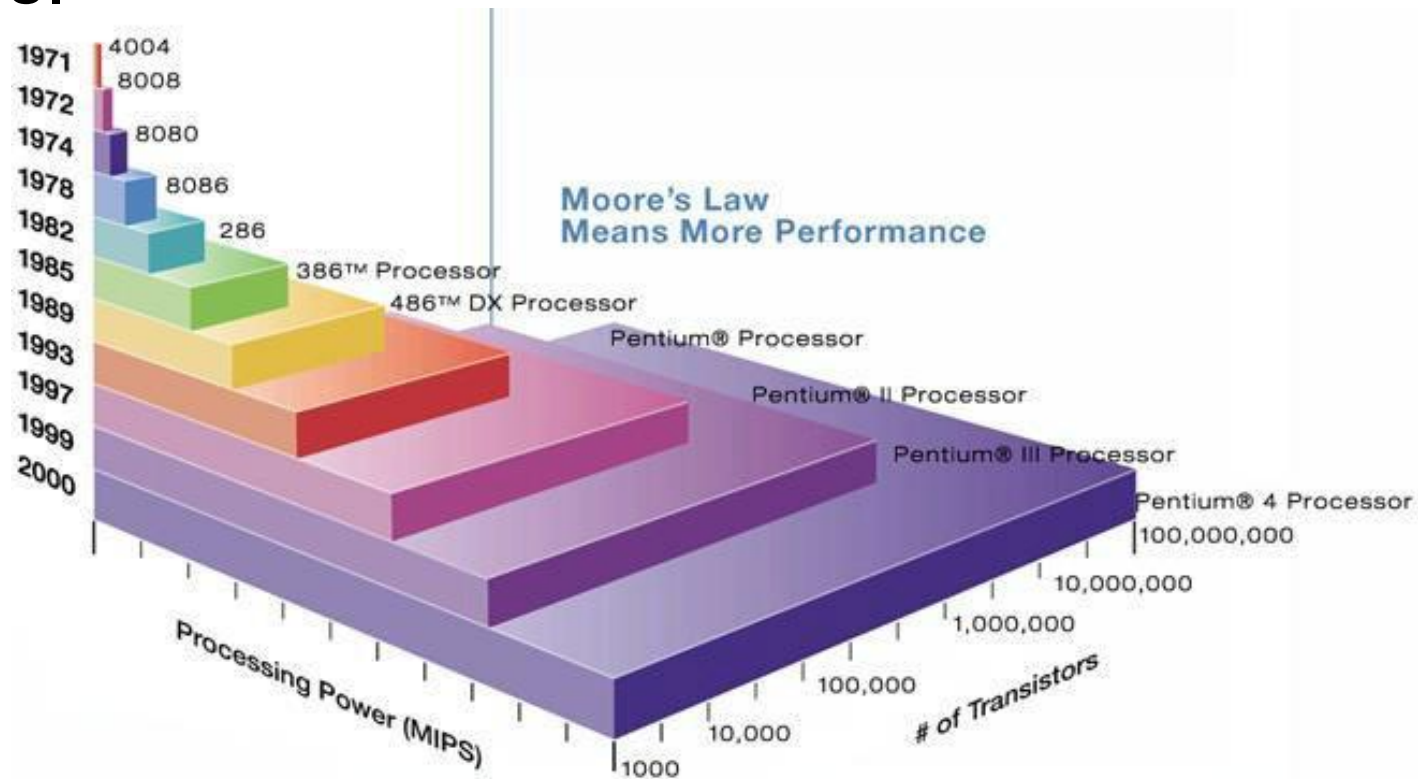
# Integration Levels

- Gate/transistor ratio is roughly 1/10
  - SSI < 12 gates/chip
  - MSI < 100 gates/chip
  - LSI ... 1K gates/chip
  - VLSI ... 10K gates/chip
  - ULSI ... 100K gates/chip
  - GSI ... 1Meg gates/chip



# Moore's law

- A prediction made by Moore (a co-founder of Intel) in 1965: "... a number of transistors to double every 2 years."



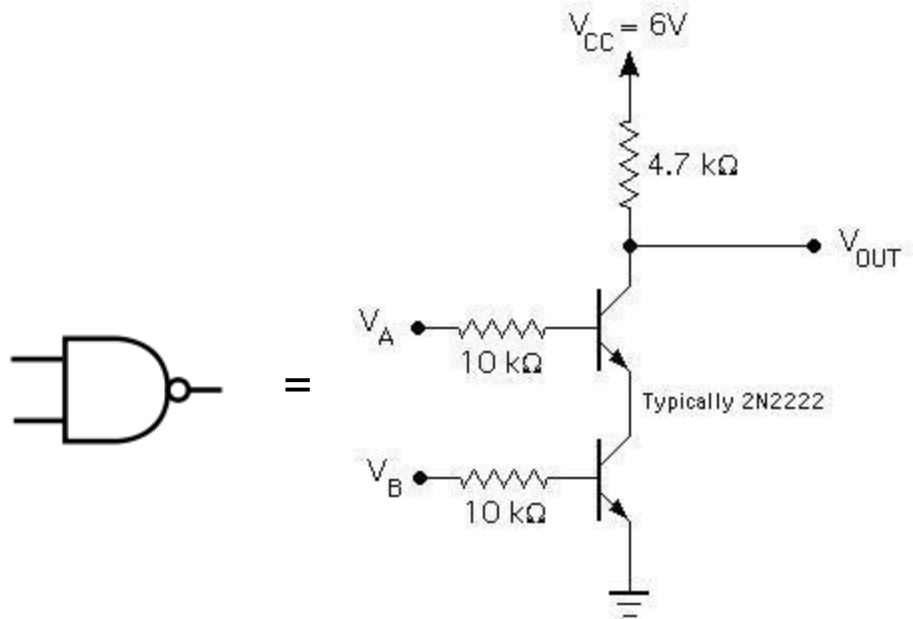
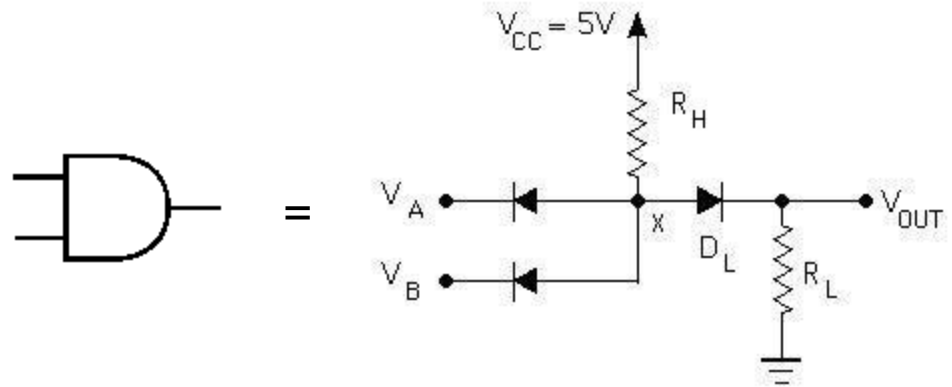
# In the beginning...

## Diode Logic (DL)

- simplest; does not scale
- NOT not possible (need an active element).

## Transistor Logic (RTL)

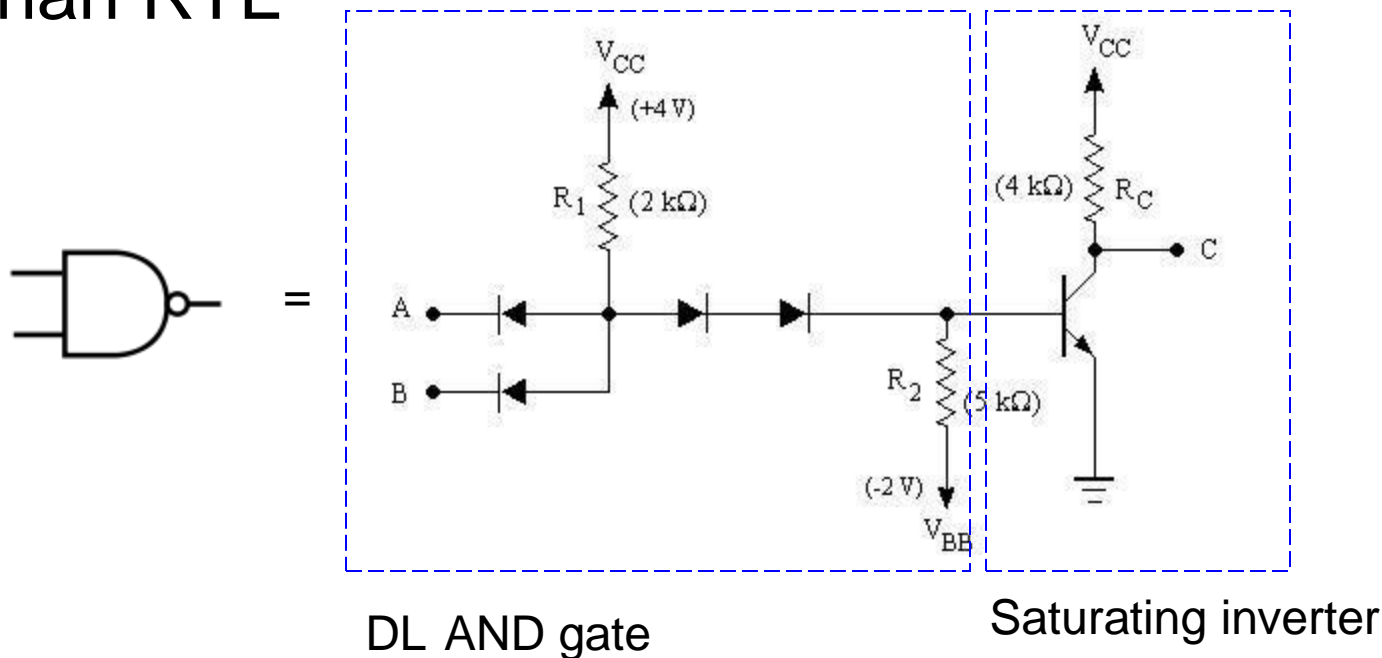
- replace diode switch with a transistor switch
- can be cascaded
- large power draw



# was...

## Diode-Transistor Logic (DTL)

- essentially diode logic with transistor amplification
- reduced power consumption
- faster than RTL



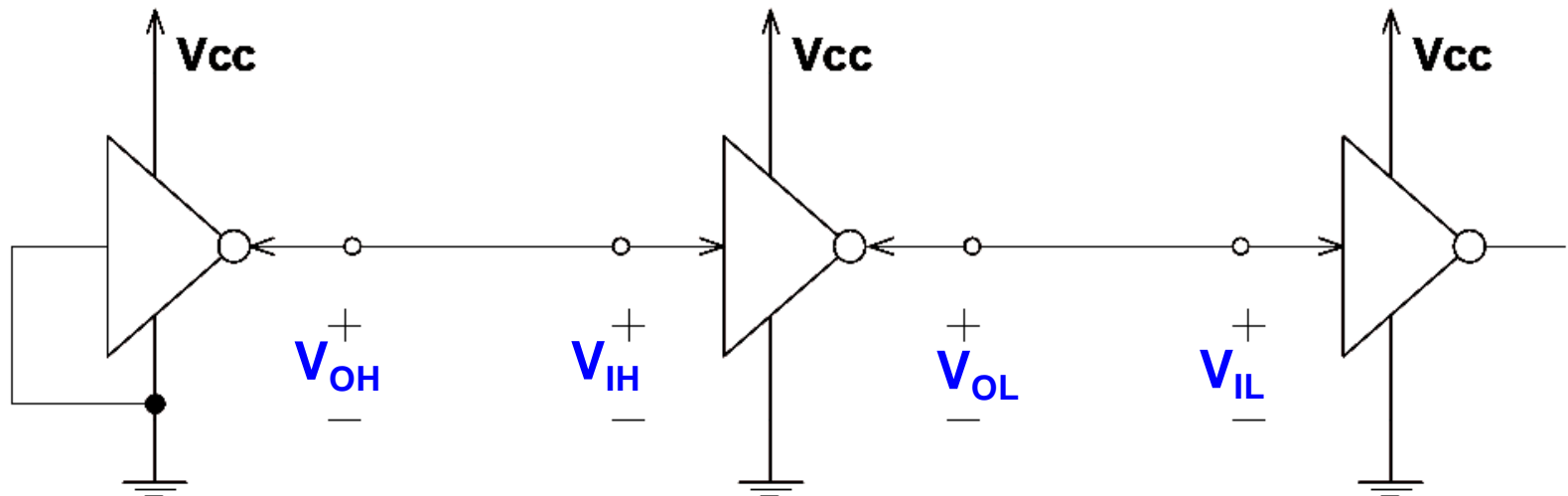
# Logic families: V levels

$V_{OH}(\text{min})$  – The minimum voltage level at an output in the logical “1” state under defined load conditions

$V_{OL}(\text{max})$  – The maximum voltage level at an output in the logical “0” state under defined load conditions

$V_{IH}(\text{min})$  – The minimum voltage required at an input to be recognized as “1” logical state

$V_{IL}(\text{max})$  – The maximum voltage required at an input that still will be recognized as “0” logical state



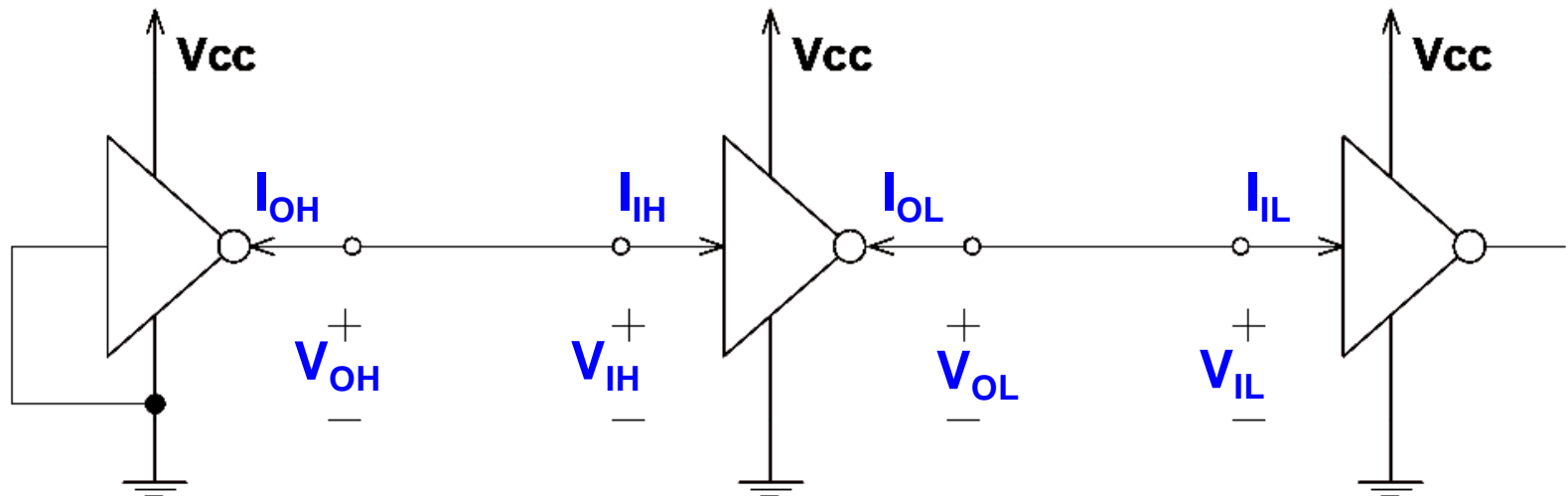
# Logic families: I requirements

$I_{OH}$  – Current flowing into an output in the logical “1” state under specified load conditions

$I_{OL}$  – Current flowing into an output in the logical “0” state under specified load conditions

$I_{IH}$  – Current flowing into an input when a specified HI level is applied to that input

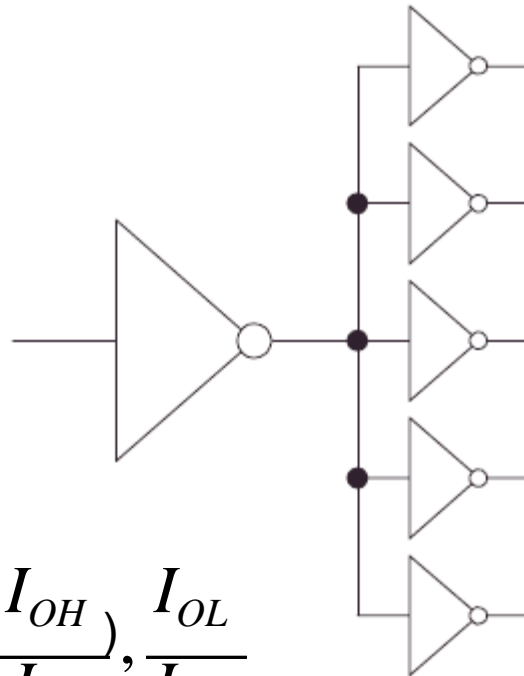
$I_{IL}$  – Current flowing into an input when a specified LO level is applied to that input





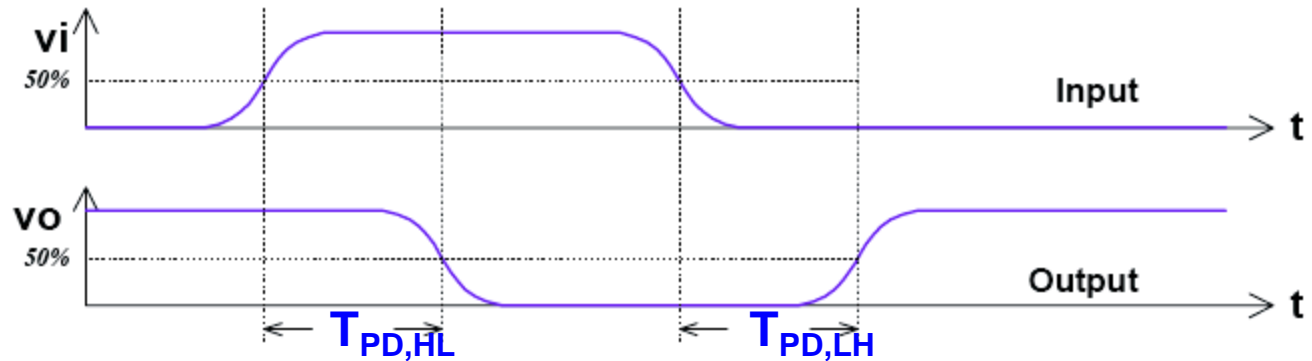
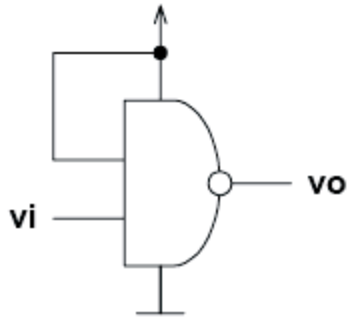
# Logic families: fanout

Fanout: the maximum number of logic inputs (of the same logic family) that an output can drive reliably



$$\text{DC fanout} = \min\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

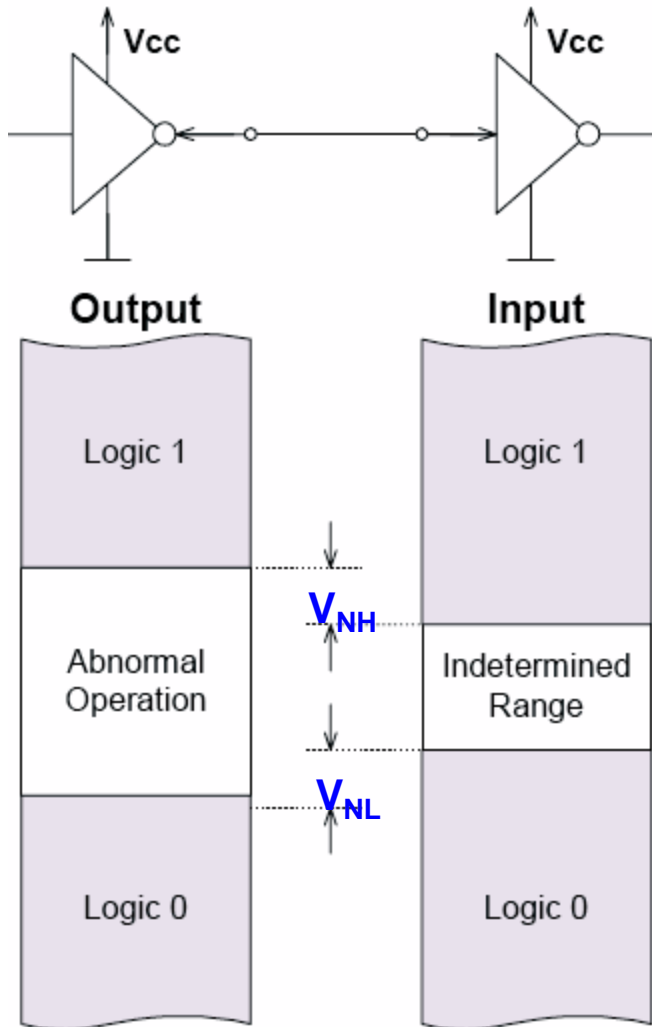
# Logic families: propagation delay



$T_{PD,HL}$  – input-to-output propagation delay from HI to LO output  
 $T_{PD,LH}$  – input-to-output propagation delay from LO to HI output

Speed-power product:  $T_{PD} \times P_{avg}$

# Logic families: noise margin



HI state noise margin:

$$V_{NH} = V_{OH}(\min) - V_{IH}(\min)$$

LO state noise margin:

$$V_{NL} = V_{IL}(\max) - V_{OL}(\max)$$

Noise margin:

$$V_N = \min(V_{NH}, V_{NL})$$

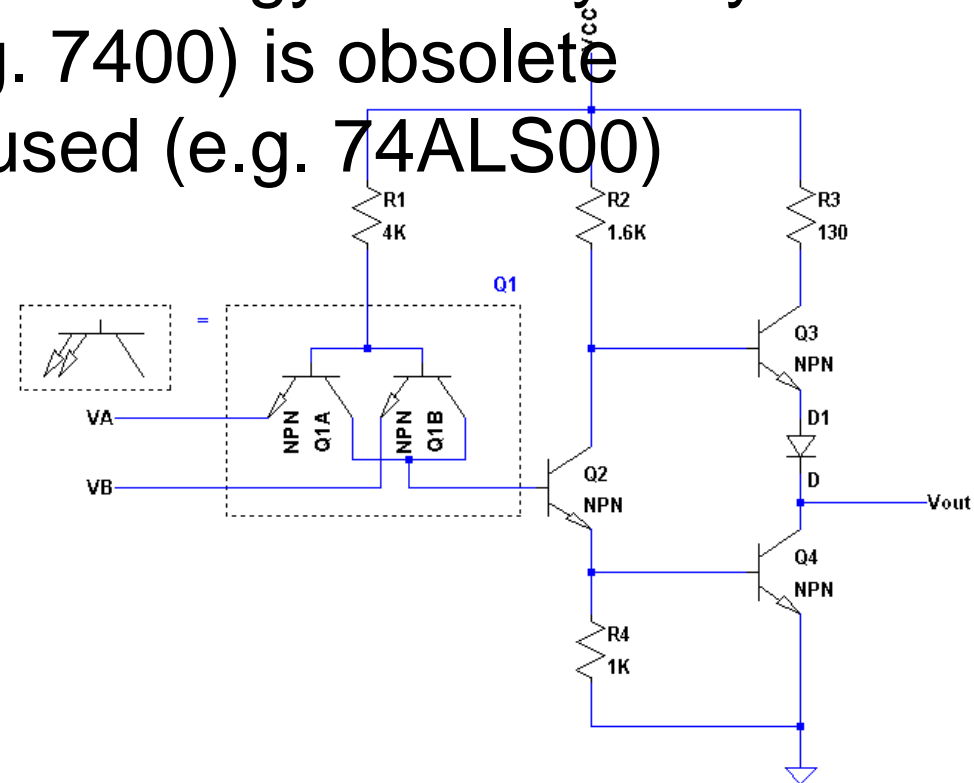
# TTL

## Bipolar Transistor-Transistor Logic (TTL)

- first introduced by in 1964 (Texas Instruments)
- TTL has shaped digital technology in many ways
- Standard TTL family (e.g. 7400) is obsolete
- Newer TTL families still used (e.g. 74ALS00)

## Distinct features

- Multi-emitter transistors
- Totem-pole transistor arrangement
- Open LTspice example:  
TTL NAND...

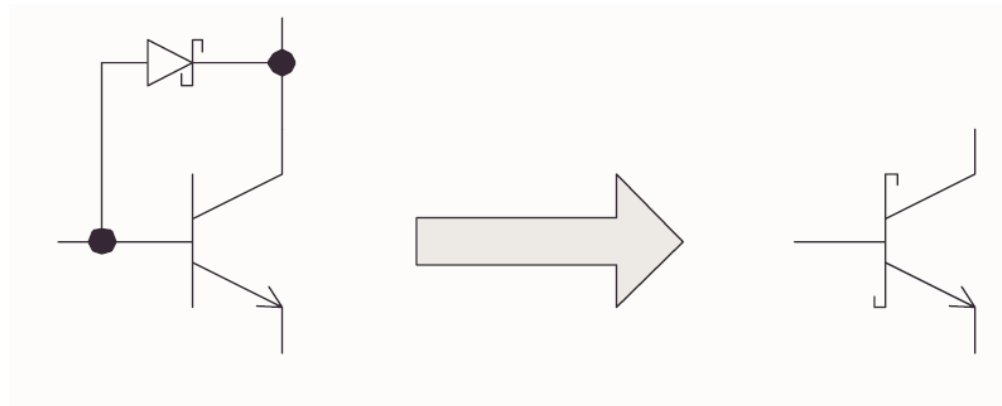


2-input NAND

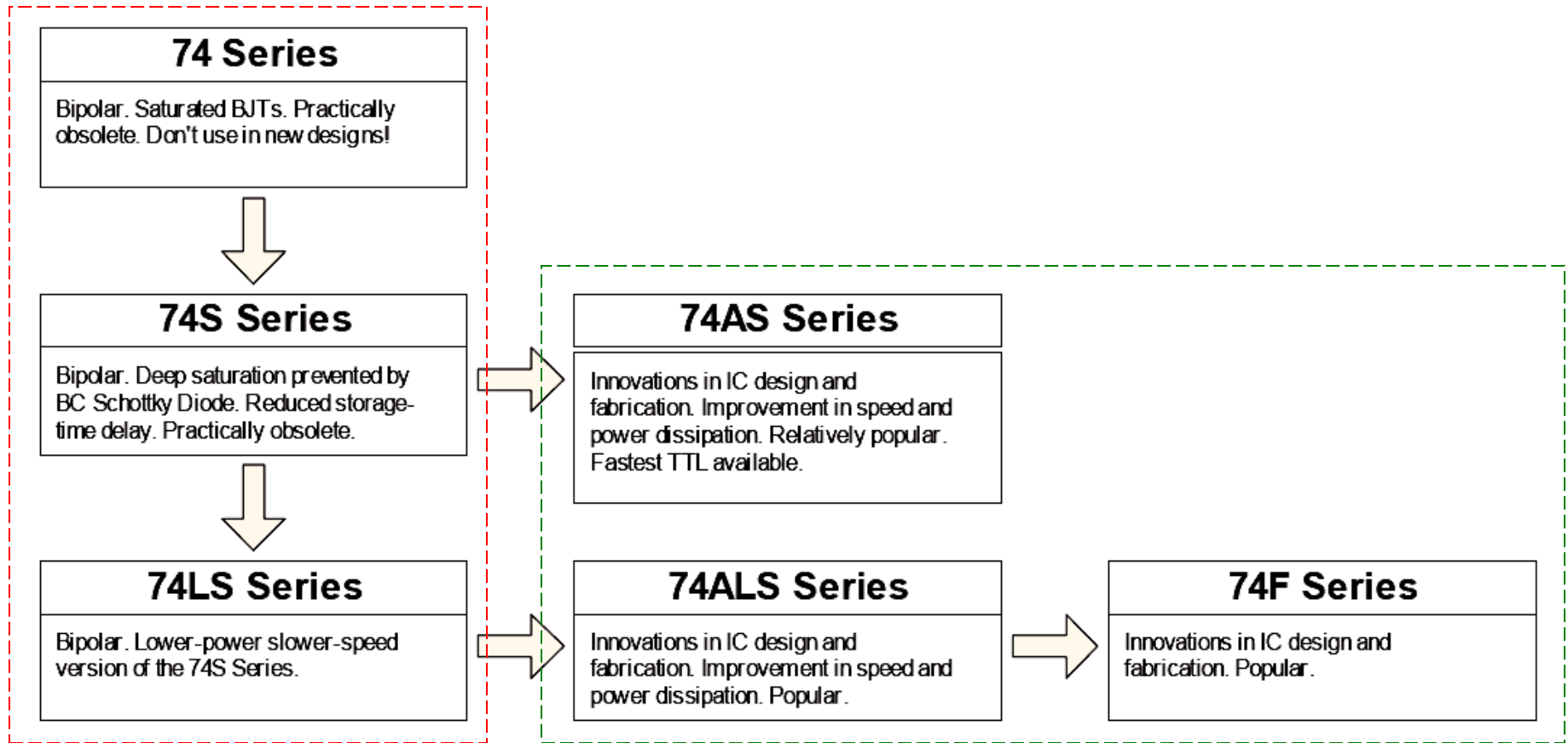
# TTL evolution

## Schottky series (74LS00) TTL

- A major slowdown factor in BJTs is due to transistors going in/out of saturation
- Schottky diode has a lower forward bias (0.25V)
- When BC junction would become forward biased, the Schottky diode bypasses the current preventing the transistor from going into saturation



# TTL family evolution



Legacy: don't use in new designs

Widely used today

# ECL

## Emitter-Coupled Logic (ECL)

- PROS: Fastest logic family available ( $\sim 1\text{ns}$ )
- CONS: low noise margin and high power dissipation
- Operated in emitter coupled geometry (recall differential amplifier or emitter-follower), transistors are biased and operate near their Q-point (never near saturation!)
- Logic levels. “0”:  $-1.7\text{V}$ . “1”:  $-0.8\text{V}$
- Such strange logic levels require extra effort when interfacing to TTL/CMOS logic families.
- Open LTspice example: ECL inverter...

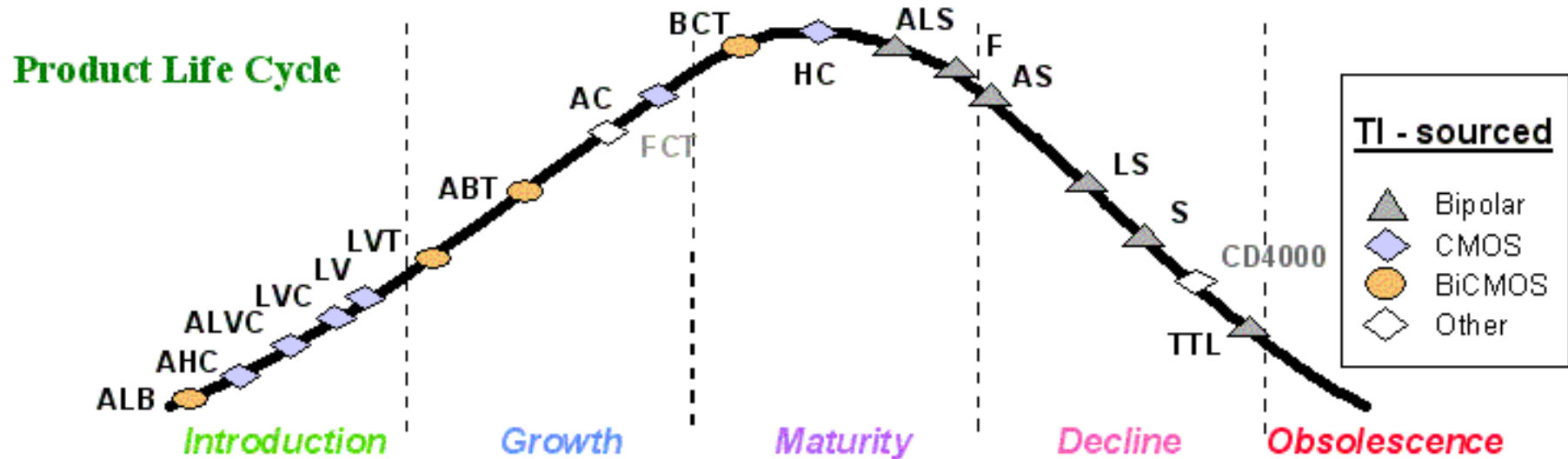
# CMOS

## Complimentary MOS (CMOS)

- Other variants: NMOS, PMOS (obsolete)
- Very low static power consumption
- Scaling capabilities (large integration all MOS)
- Full swing: rail-to-rail output
- Things to watch out for:
  - don't leave inputs floating (in TTL these will float to HI, in CMOS you get undefined behaviour)
  - susceptible to electrostatic damage (finger of death)



# Life-cycle



A decorative graphic on the left side of the slide consists of several overlapping squares in various shades of blue and purple, arranged in a stepped pattern. A solid dark blue horizontal bar spans the width of the slide, positioned above the text. At the top center, there is a thin, light gray horizontal bar.

# Combinational Circuits



# Outline

- Boolean Algebra
- Decoder
- Encoder
- MUX

# History: Computer and the Rationalist

- Modern research issues in AI are formed and evolve through a combination of historical, social and cultural pressures.
- The rationalist tradition had an early proponent in Plato, and was continued on through the writings of Pascal, Descartes, and Leibniz
- For the rationalist, the external world is reconstructed through the clear and distinct ideas of a mathematics

# History: Development of Formal Logic

- The goal of creating a formal language for thought also appears in the work of George Boole, another 19<sup>th</sup> century mathematician whose work must be included in the roots of AI
- The importance of Boole's accomplishment is in the extraordinary power and simplicity of the system he devised: **Three Operations**

# Three Operations

- **three basic Boolean operations** can be defined arithmetically as follows.

- $x \wedge y = xy$

- $x \vee y = x + y - xy$

- $\neg x = 1 - x$

Figure 1. Truth tables

$x$	$y$	$x \wedge y$	$x \vee y$	$x$	$\neg x$
0	0	0	0	0	1
1	0	0	1	1	0
0	1	0	1		
1	1	1	1		

# Boolean function and logic diagram

- **Boolean algebra:** Deals with binary variables and logic operations operating on those variables.
- **Logic diagram:** Composed of graphic symbols for logic gates. A simple circuit sketch that represents inputs and outputs of Boolean functions.

# *Basic Identities of Boolean Algebra*

$$(1) \quad x + 0 = x$$

$$(2) \quad x \cdot 0 = 0$$

$$(3) \quad x + 1 = 1$$

$$(4) \quad x \cdot 1 = x$$

$$(5) \quad x + x = x$$

$$(6) \quad x \cdot x = x$$

$$(7) \quad x + x' = 1$$

$$(8) \quad x \cdot x' = 0$$

$$(9) \quad x + y = y + x$$

$$(10) \quad xy = yx$$

$$(11) \quad x + (y + z) = (x + y) + z$$

$$(12) \quad x(yz) = (xy)z$$

$$(13) \quad x(y + z) = xy + xz$$

$$(14) \quad x + yz = (x + y)(x + z)$$

$$(15) \quad (x + y)' = x' y'$$

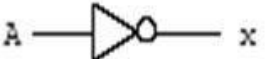
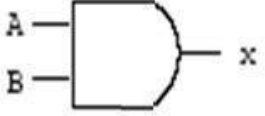
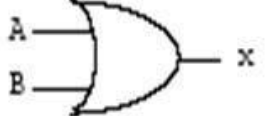
$$(16) \quad (xy)' = x' + y'$$

$$(17) \quad (x')' = x$$



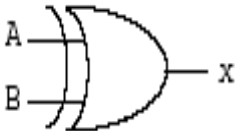
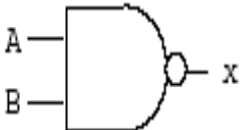
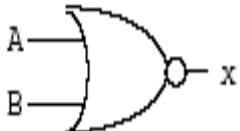
# Gates

- Refer to the hardware to implement Boolean operators.
- The most basic gates are

Name	Graphic symbol	Algebraic function	Truth table															
Inverter		$x = A'$	<table border="1"> <tr><td>A</td><td>x</td></tr> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </table>	A	x	0	1	1	0									
A	x																	
0	1																	
1	0																	
AND		$x = AB$	<table border="1"> <tr><td>A</td><td>B</td><td>x</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table> <p>True if both are true.</p>	A	B	x	0	0	0	0	1	0	1	0	0	1	1	1
A	B	x																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$x = A + B$	<table border="1"> <tr><td>A</td><td>B</td><td>x</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table> <p>True if either one is true.</p>	A	B	x	0	0	0	0	1	1	1	0	1	1	1	1
A	B	x																
0	0	0																
0	1	1																
1	0	1																
1	1	1																

# Boolean function and truth table

- Other common gates include:

Name	Graphic symbol	Algebraic function	Truth table															
Exclusive-OR (XOR)		$x = A \oplus B$ $= A'B + AB'$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>x</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	x	0	0	0	0	1	1	1	0	1	1	1	0
A	B	x																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
NAND		$x = (AB)'$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>x</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	x	0	0	1	0	1	1	1	0	1	1	1	0
A	B	x																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$x = A + B$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>x</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	x	0	0	1	0	1	0	1	0	0	1	1	0
A	B	x																
0	0	1																
0	1	0																
1	0	0																
1	1	0																

Parity check: True if only one is true.

Inversion of AND.

Inversion of OR.



# Outline

- Boolean Algebra
- Decoder
- Encoder
- MUX

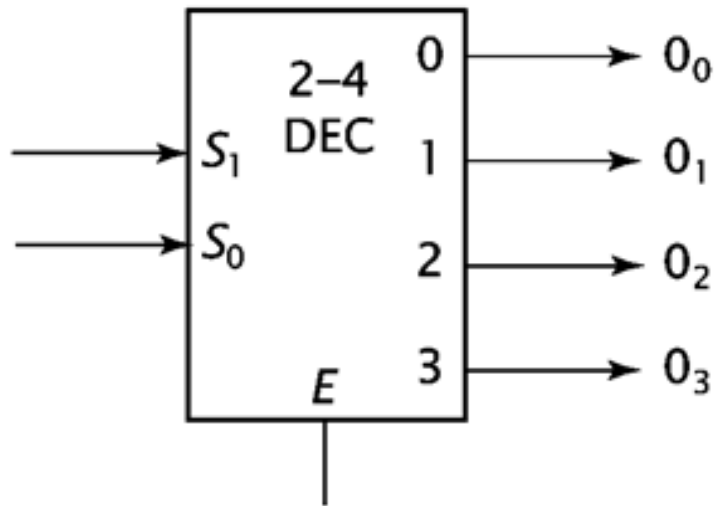
# Decoder

- **Accepts a value and decodes it**
  - **Output corresponds to value of  $n$  inputs**
  
- **Consists of:**
  - **Inputs ( $n$ )**
  - **Outputs ( $2^n$  , numbered from  $0 \rightarrow 2^n - 1$ )**
  - **Selectors / Enable (active high or active low)**

# The truth table of 2-to-4 Decoder

$S_1$	$S_0$	$E$	$O_0$	$O_1$	$O_2$	$O_3$
X	X	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

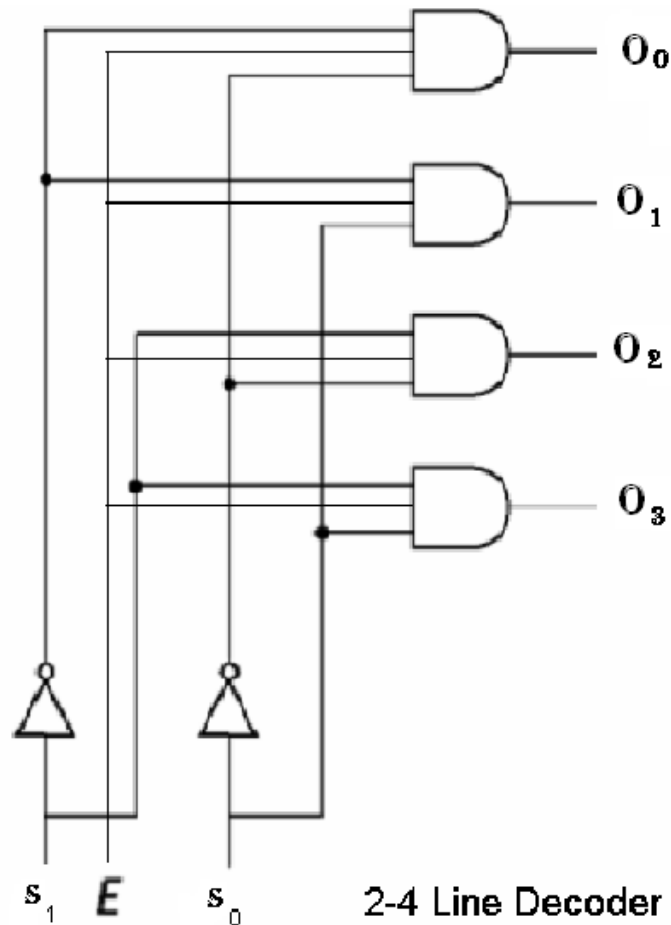
# 2-to-4 Decoder



$S_1$	$S_0$	$E$	$O_0$	$O_1$	$O_2$	$O_3$
X	X	0	0	0	0	0
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

(b)

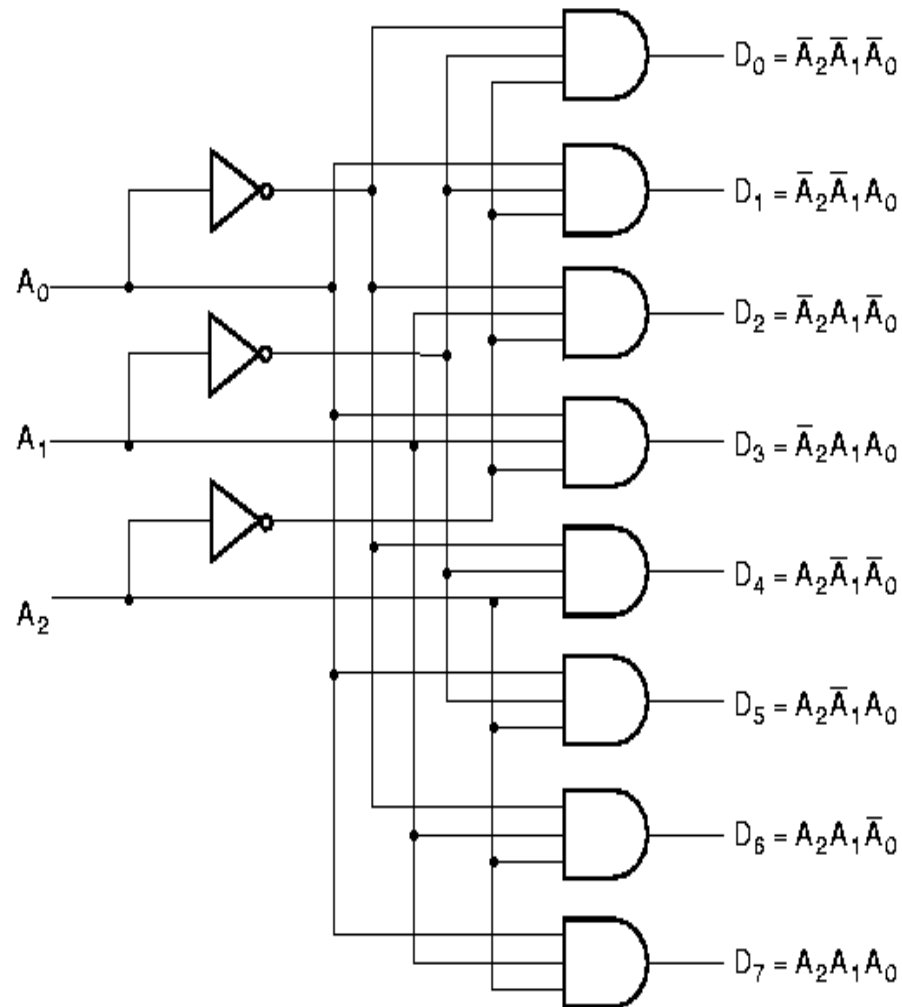
# 2-to-4 Decoder



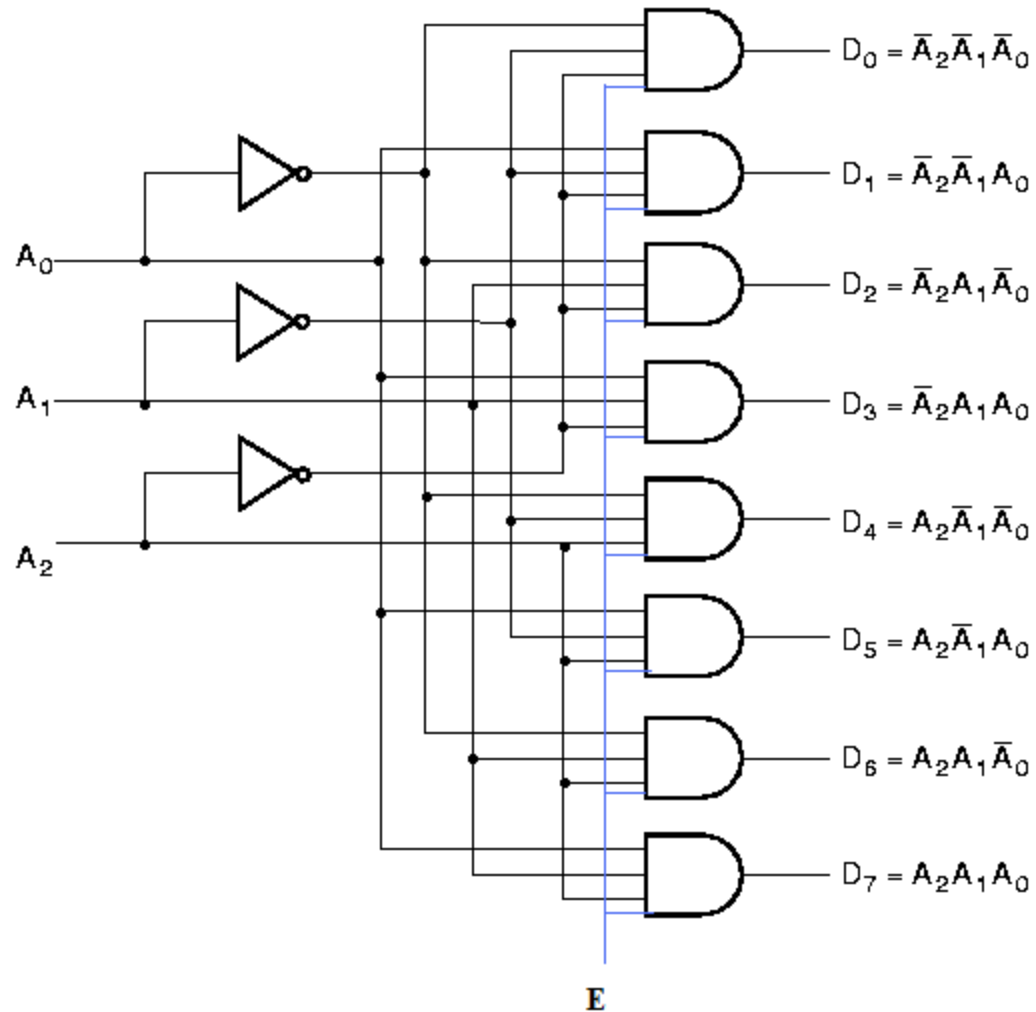




# 3-to-8 Decoder



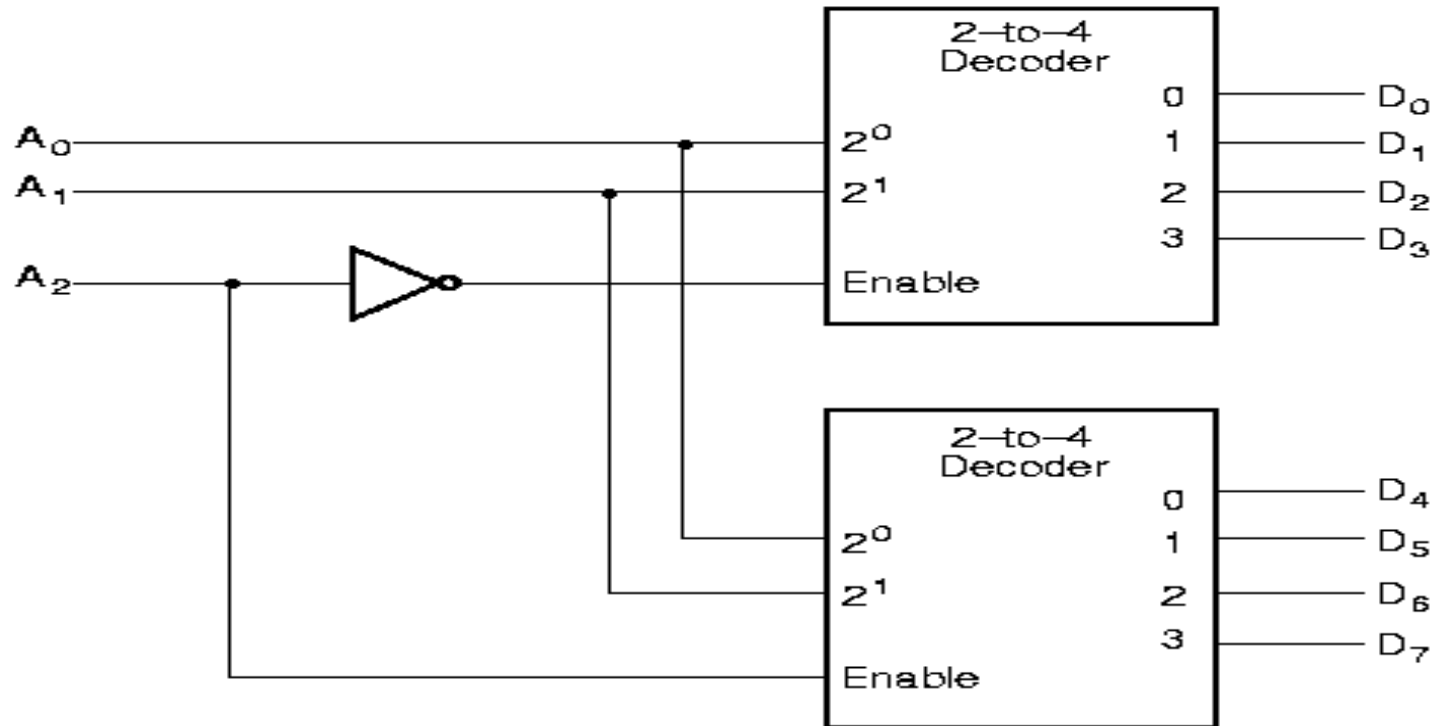
# 3-to-8 Decoder with Enable



# Decoder Expansion

- Decoder expansion
- Combine two or more small decoders with enable inputs to form a larger decoder
- 3-to-8-line decoder constructed from two 2-to-4-line decoders
  - The MSB is connected to the enable inputs
  - if  $A_2=0$ , upper is enabled; if  $A_2=1$ , lower is enabled.

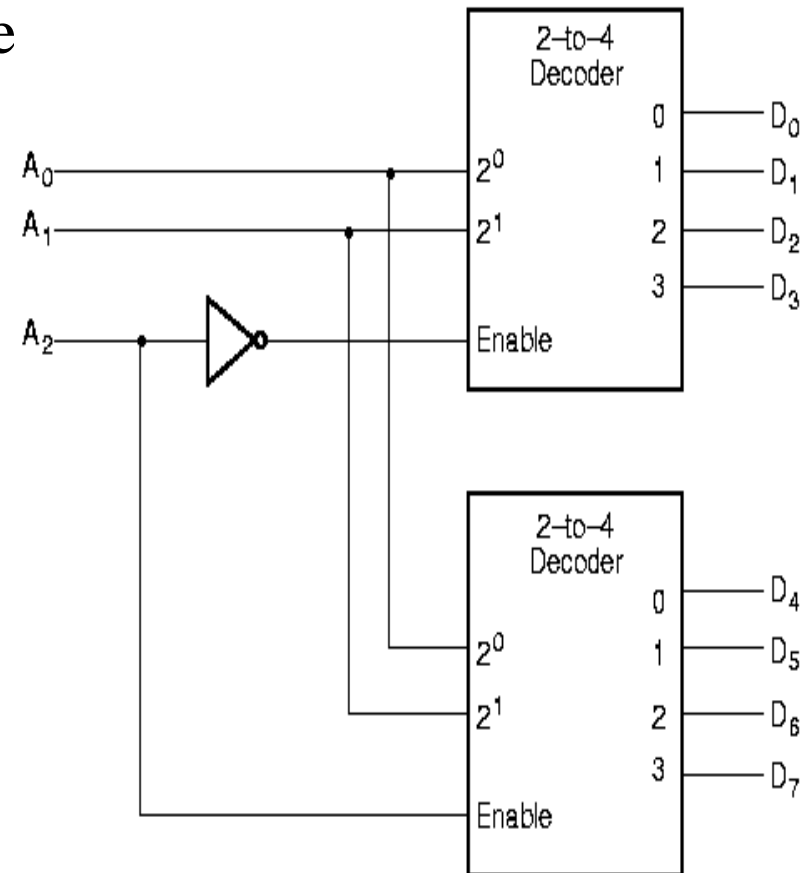
# Decoder Expansion



# Combining two 2-4 decoders to form one 3-8 decoder using enable switch

$A_2$	$A_1$	$A_0$	$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

e



The highest bit is used for the enable

# How about 4-16 decoder

- Use how many 3-8 decoder?
- Use how many 2-4 decoder?



# Outline

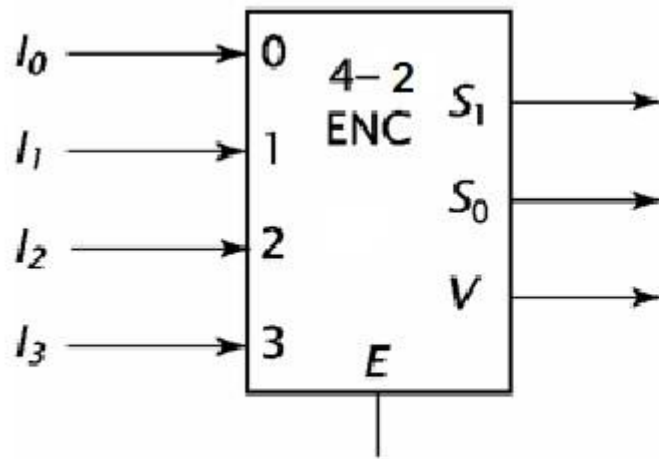
- Boolean Algebra
- Decoder
- Encoder
- Mux

# Encoders

- Perform the inverse operation of a decoder
  - $2^n$  (or less) input lines and  $n$  output lines

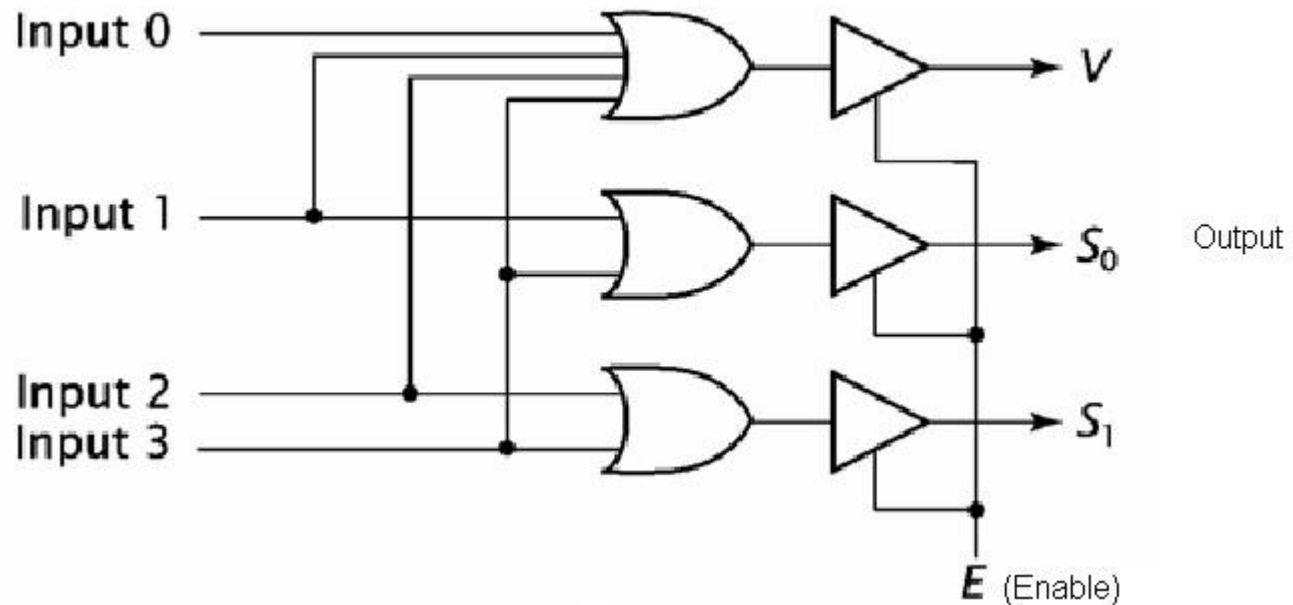


# Encoders



$I_0$	$I_1$	$I_2$	$I_3$	$E$	$S_1$	$S_0$	$V$
X	X	X	X	0	Z	Z	Z
0	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1
0	1	0	0	1	0	1	1
0	0	1	0	1	1	0	1
0	0	0	1	1	1	1	1

# Encoders with OR gates



# Encoders

- Perform the inverse operation of a decoder
  - $2^n$  (or less) input lines and  $n$  output lines

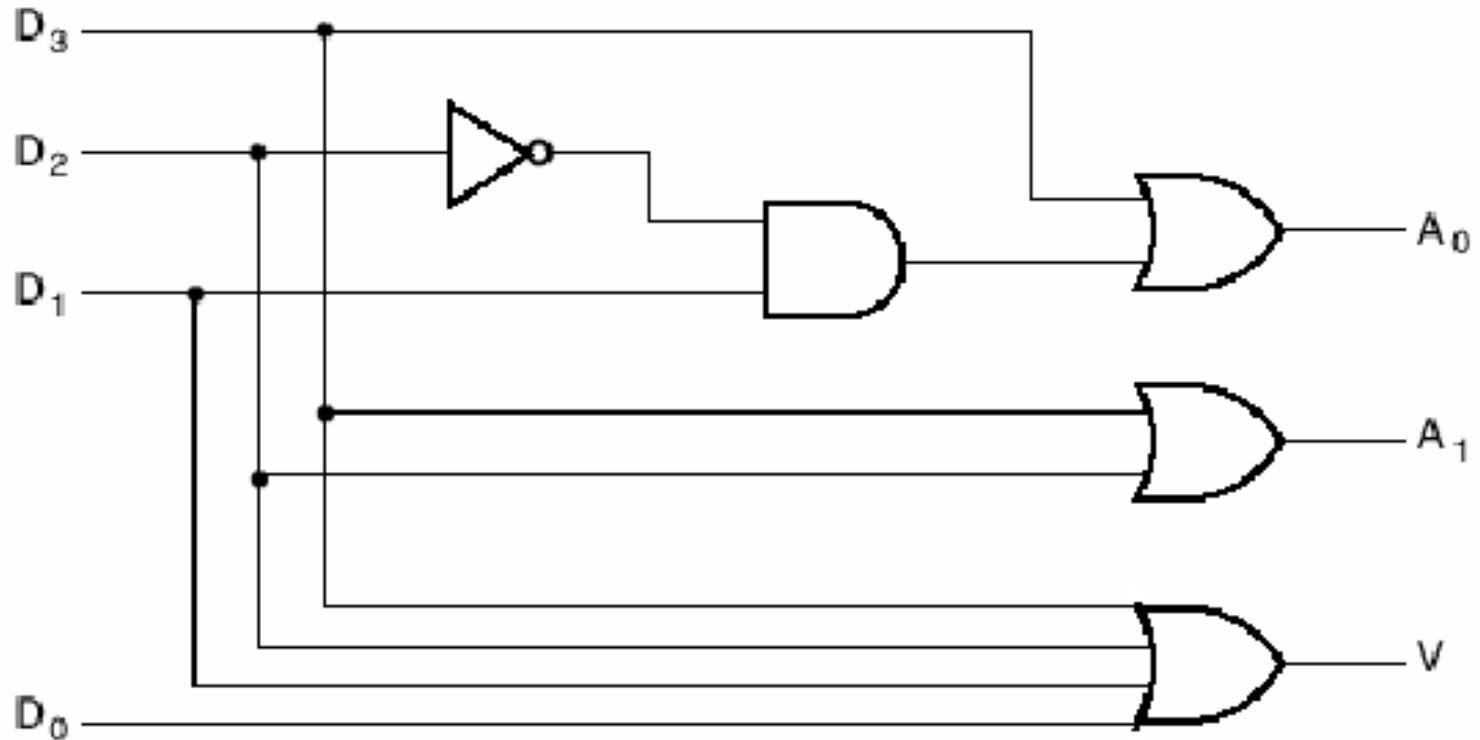
<b>D<sub>7</sub></b>	<b>D<sub>6</sub></b>	<b>D<sub>5</sub></b>	<b>D<sub>4</sub></b>	<b>D<sub>3</sub></b>	<b>D<sub>2</sub></b>	<b>D<sub>1</sub></b>	<b>D<sub>0</sub></b>	<b>A<sub>2</sub></b>	<b>A<sub>1</sub></b>	<b>A<sub>0</sub></b>
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

# Priority Encoder

- Accepts multiple values and encodes them
  - Works when more than one input is active
- Consists of:
  - Inputs ( $2^n$ )
  - Outputs
    - when more than one output is active, sets output to correspond to highest input
    - $V$  (indicates whether any of the inputs are active)
  - Selectors / Enable (active high or active low)

D3	D2	D1	D0	A1	A0	V
0	0	0	0	x	X	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

# Priority Encoder





# Outline

- Boolean Algebra
- Decoder
- Encoder
- Mux

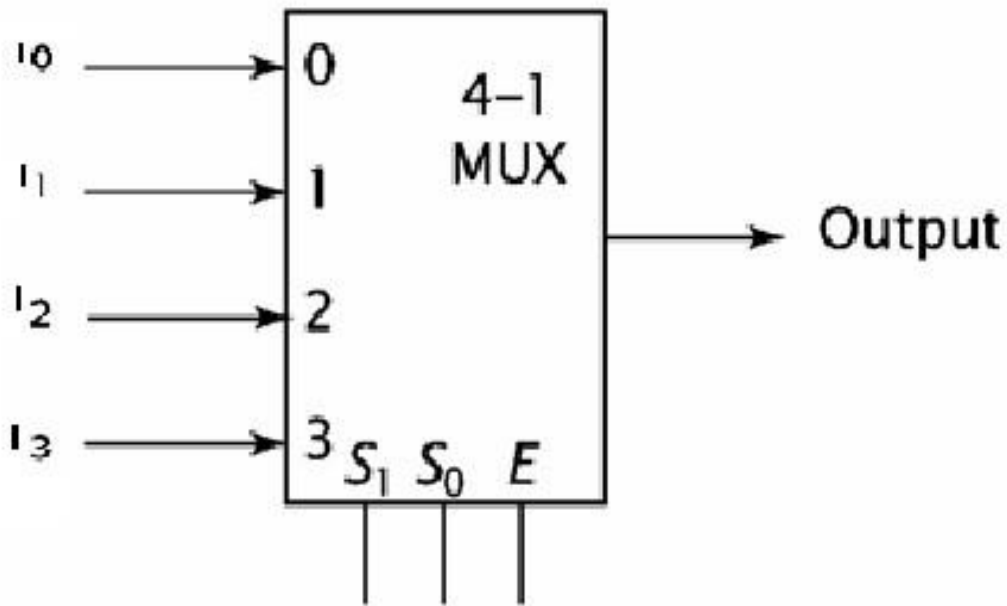
# Multiplexer (MUX)

A multiplexer can use addressing bits to select one of several input bits to be the output.

- A selector chooses a single data input and passes it to the MUX output
- It has one output selected at a time.

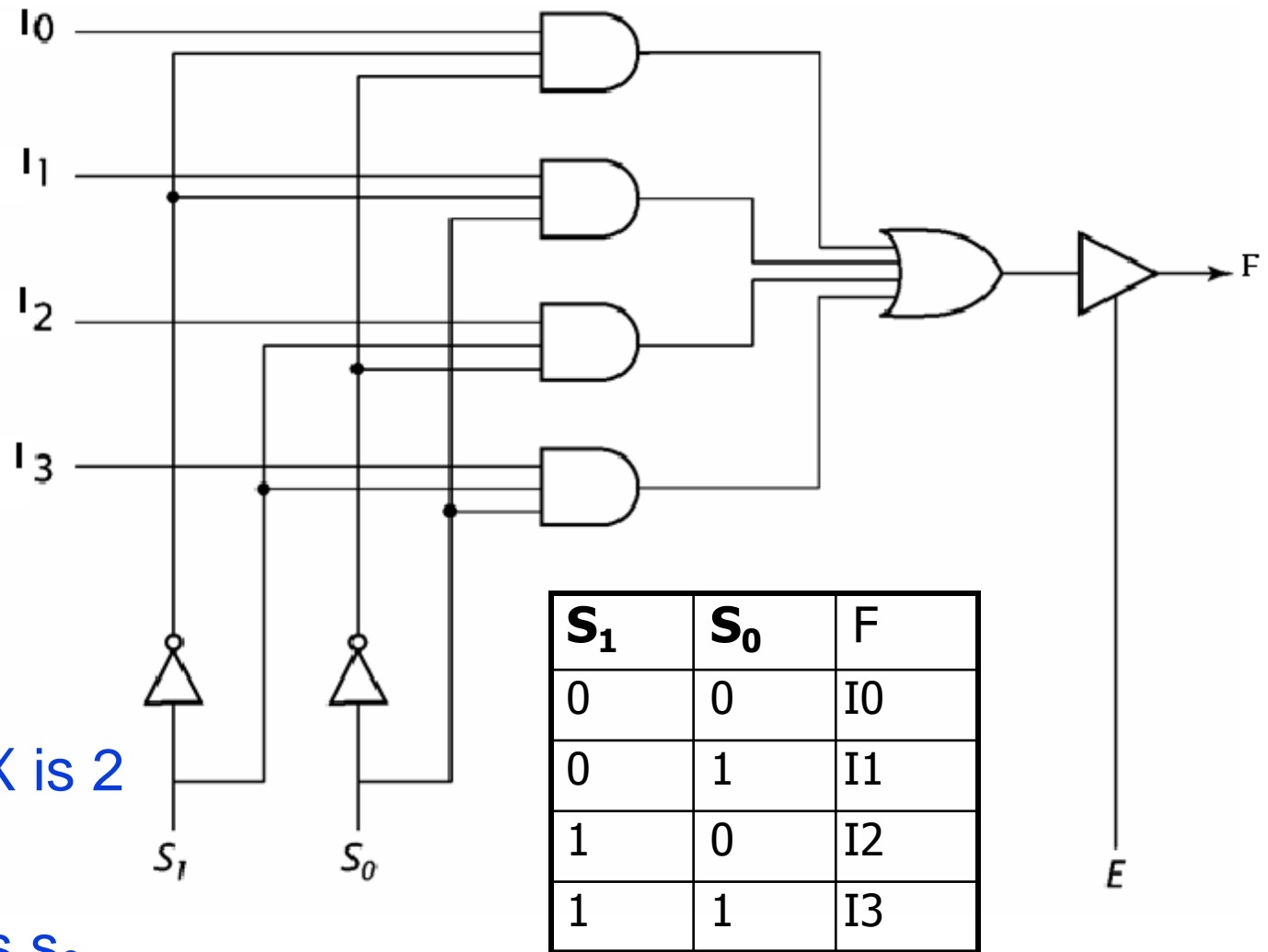


# Function table with enable



$S_1$	$S_0$	$E$	Output
X	X	0	X
0	0	1	$I_0$
0	1	1	$I_1$
1	0	1	$I_2$
1	1	1	$I_3$

# 4 to 1 line multiplexer



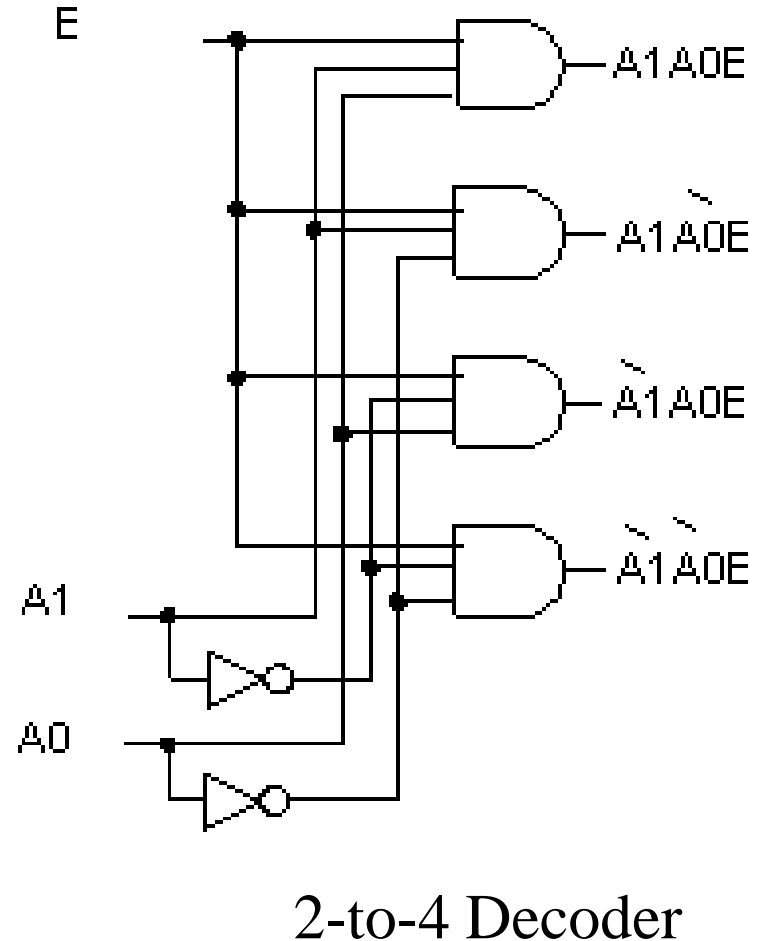
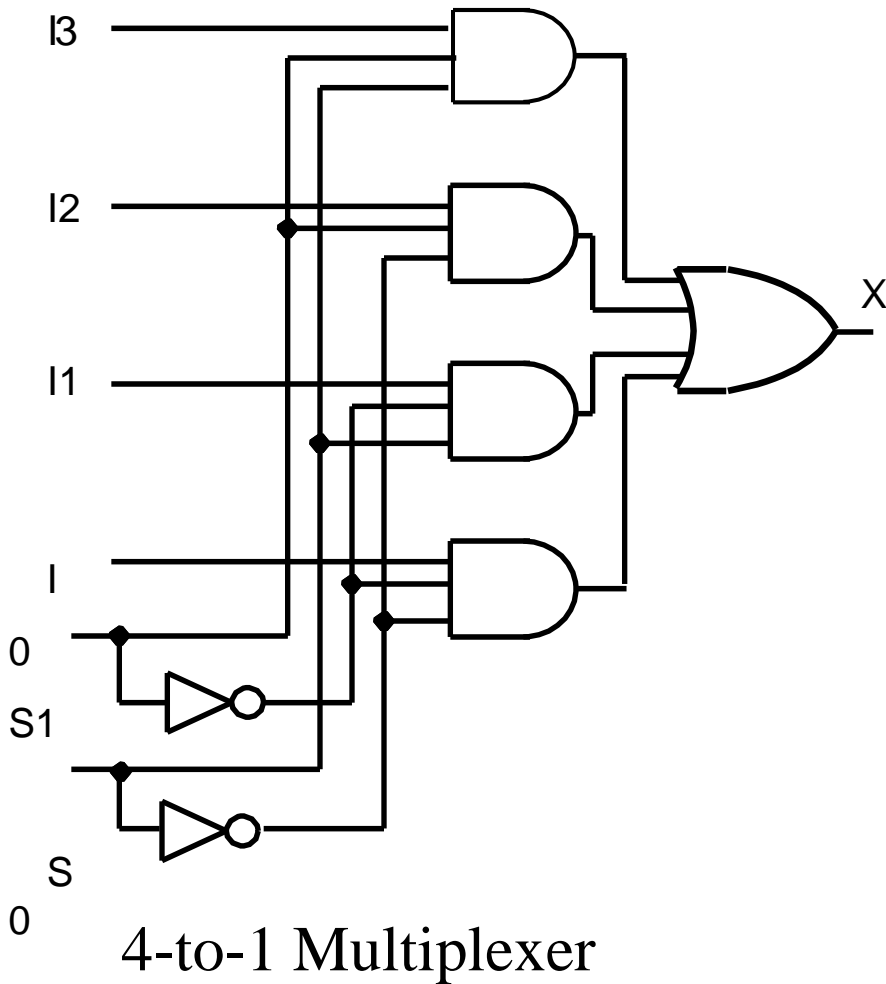
# Multiplexer (MUX)

- Consists of:
  - Inputs (multiple) =  $2^n$
  - Output (single)
  - Selectors (# depends on # of inputs) =  $n$
  - Enable (active high or active low)

# Multiplexers versus decoders

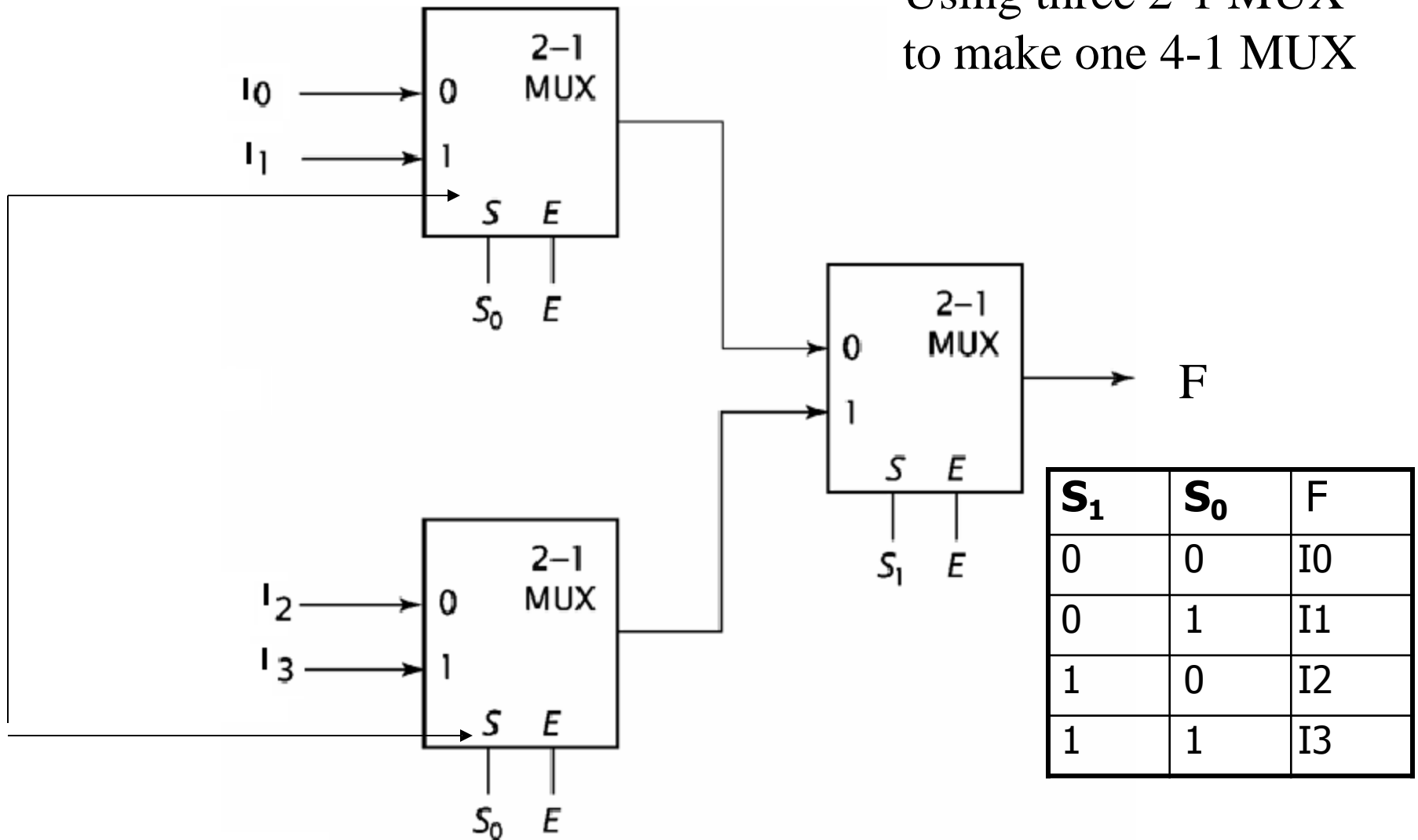
- A Multiplexer uses  $n$  binary select bits to choose from a maximum of  $2^n$  unique input lines.
- Decoders have  $2^n$  number of output lines while multiplexers have only one output line.
- The output of the multiplexer is the data input whose index is specified by the  $n$  bit code.

# Multiplexer Versus Decoder



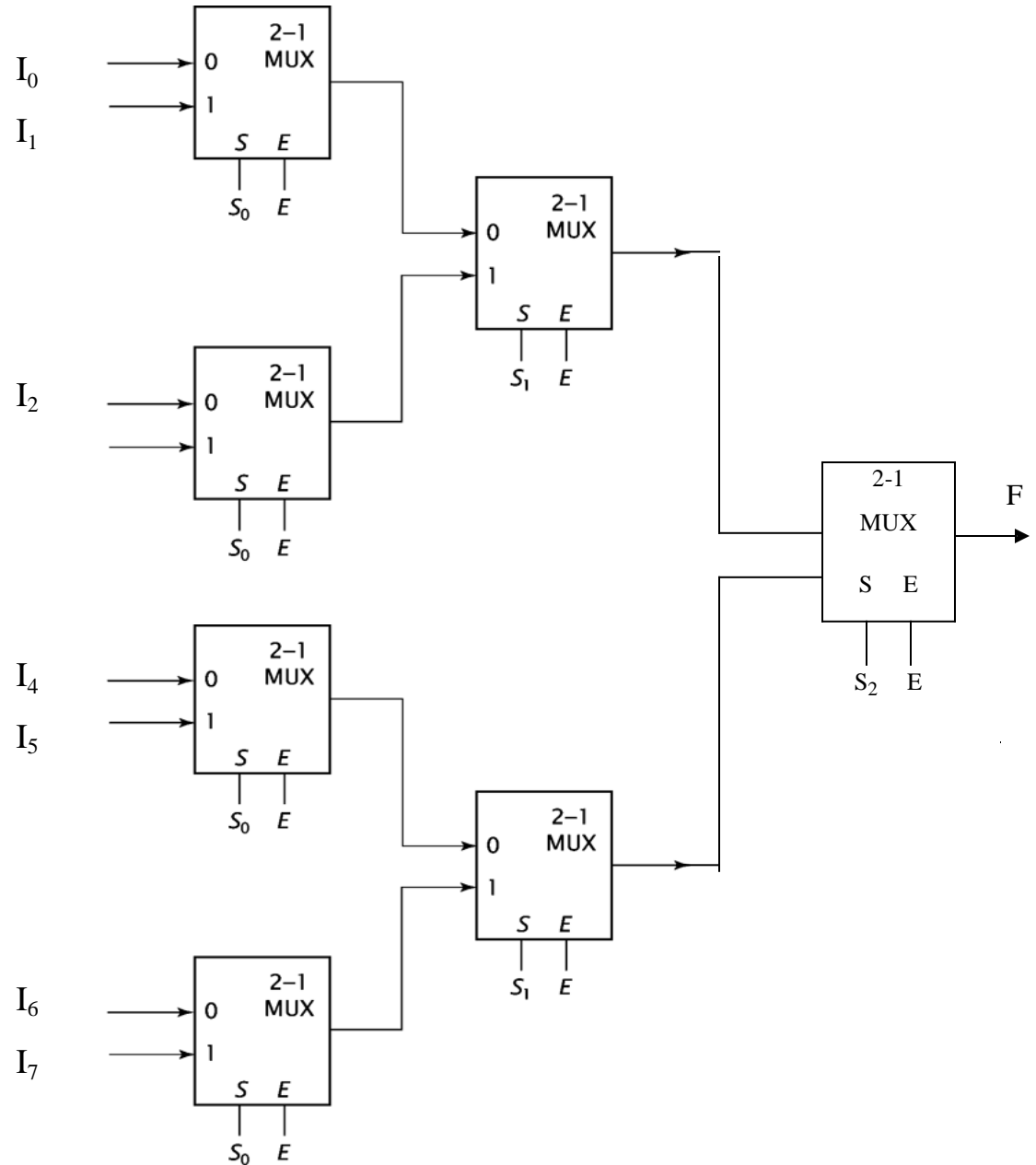
**Note that the multiplexer has an extra OR gate. A<sub>1</sub> and A<sub>0</sub> are the two inputs in decoder. There are four inputs plus two selects in multiplexer.**

# Cascading multiplexers

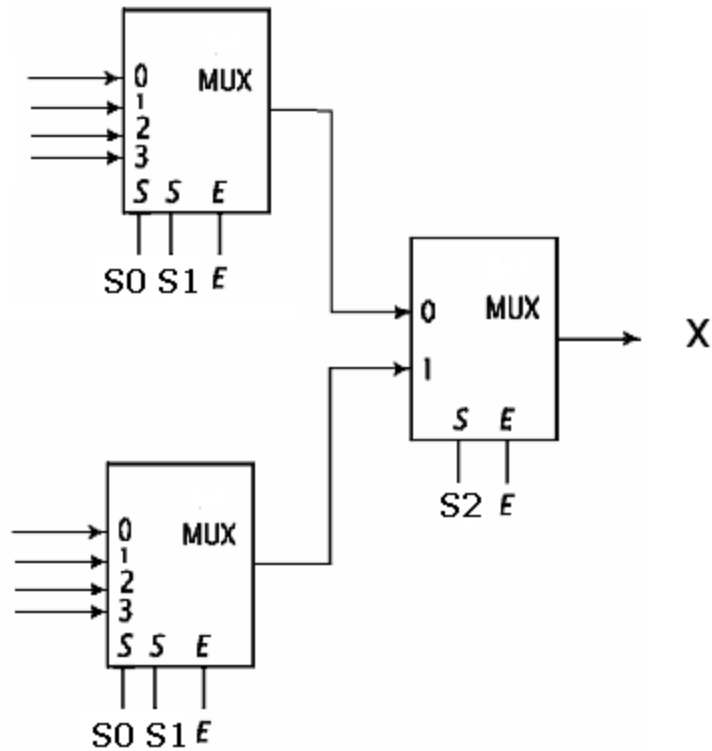


Example: Construct an 8-to-1 multiplexer using 2-to-1 multiplexers.

$S_2$	$S_1$	$S_0$	F
0	0	0	$I_0$
0	0	1	$I_1$
0	1	0	$I_2$
0	1	1	$I_3$
1	0	0	$I_4$
1	0	1	$I_5$
1	1	0	$I_6$
1	1	1	$I_7$



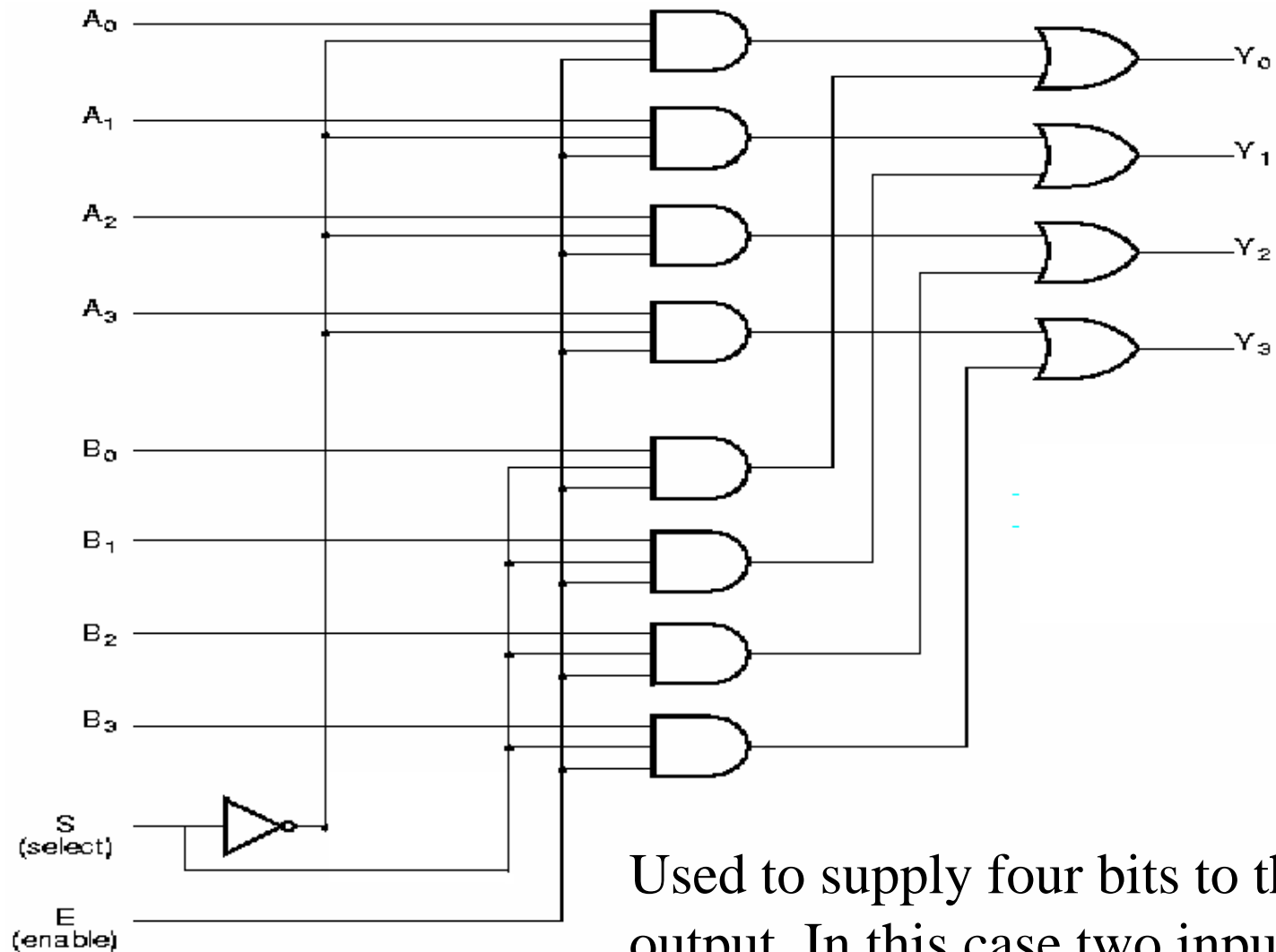
Example : Construct 8-to-1 multiplexer using one 2-to-1 multiplexer and two 4-to-1 multiplexers



$S_2$	$S_1$	$S_0$	X
0	0	0	$I_0$
0	0	1	$I_1$
0	1	0	$I_2$
0	1	1	$I_3$
1	0	0	$I_4$
1	0	1	$I_5$
1	1	0	$I_6$
1	1	1	$I_7$



# Quadruple 2-to-1 Line Multiplexer



Used to supply four bits to the output. In this case two inputs four bits each.

# Quadruple 2-to-1 Line Multiplexer

<b>E</b> <b>(Enable)</b>	<b>S</b> <b>(Select)</b>	<b>Y</b> <b>(Output)</b>
0	X	All 0's
1	0	A
1	1	B



# UNIT-5

## Sequential Circuits

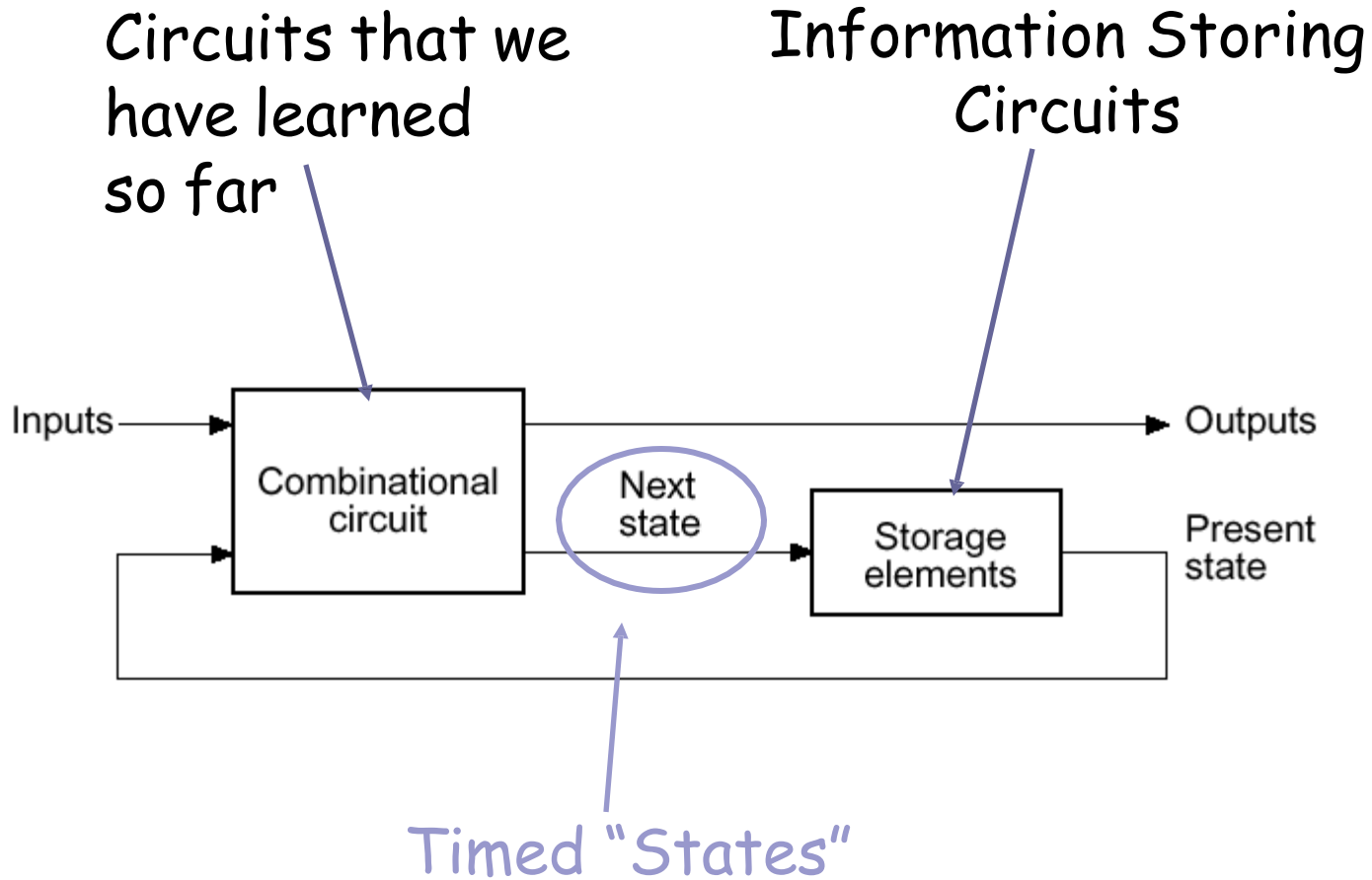
# Combinational Logic

- Combinational Logic:
  - Output depends only on current input
  - Has no memory

# Sequential Logic

- Sequential Logic:
  - Output depends not only on current input but also on past input values, e.g., design a counter
  - Need some type of memory to remember the past input values

# Sequential Circuits



# Sequential Logic: Concept

- Sequential Logic circuits remember past inputs and past circuit state.
- Outputs from the system are “fed back” as new inputs
  - With gate delay and wire delay
- The storage elements are circuits that are capable of storing binary information: memory.



# Synchronous vs. Asynchronous

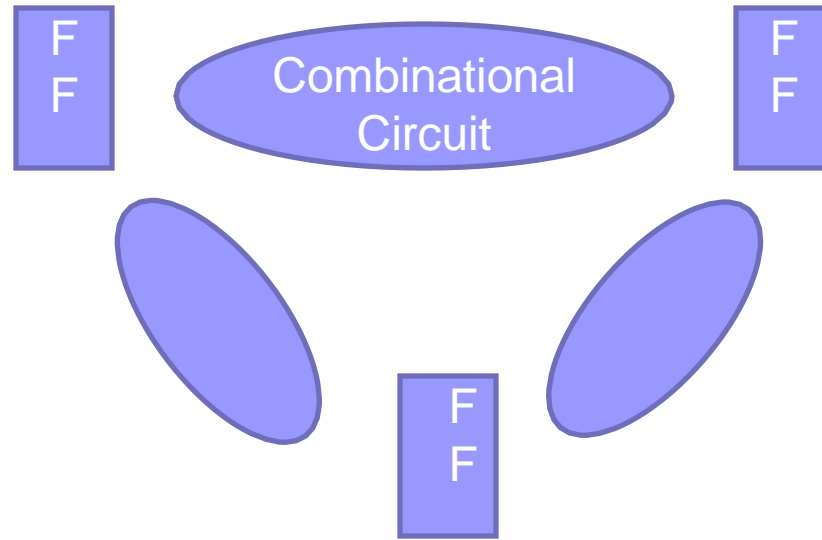
There are two types of sequential circuits:

■ **Synchronous** sequential circuit: circuit output changes only at some discrete instants of time. This type of circuits achieves synchronization by using a timing signal called the *clock*.

■ **Asynchronous** sequential circuit: circuit output can change at **any** time (clockless).

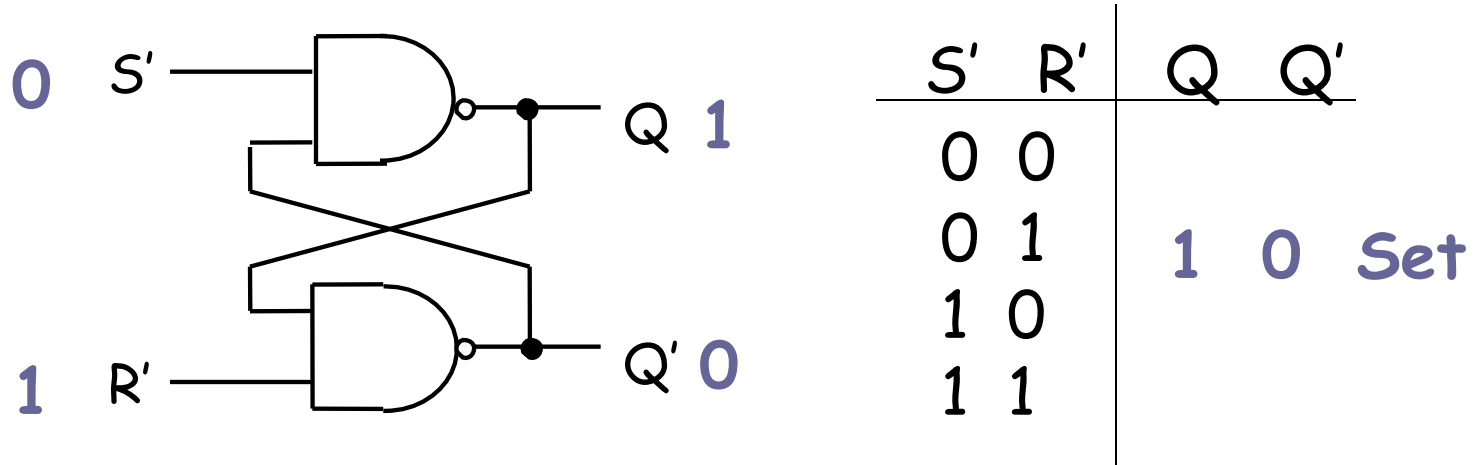


# Clock Period



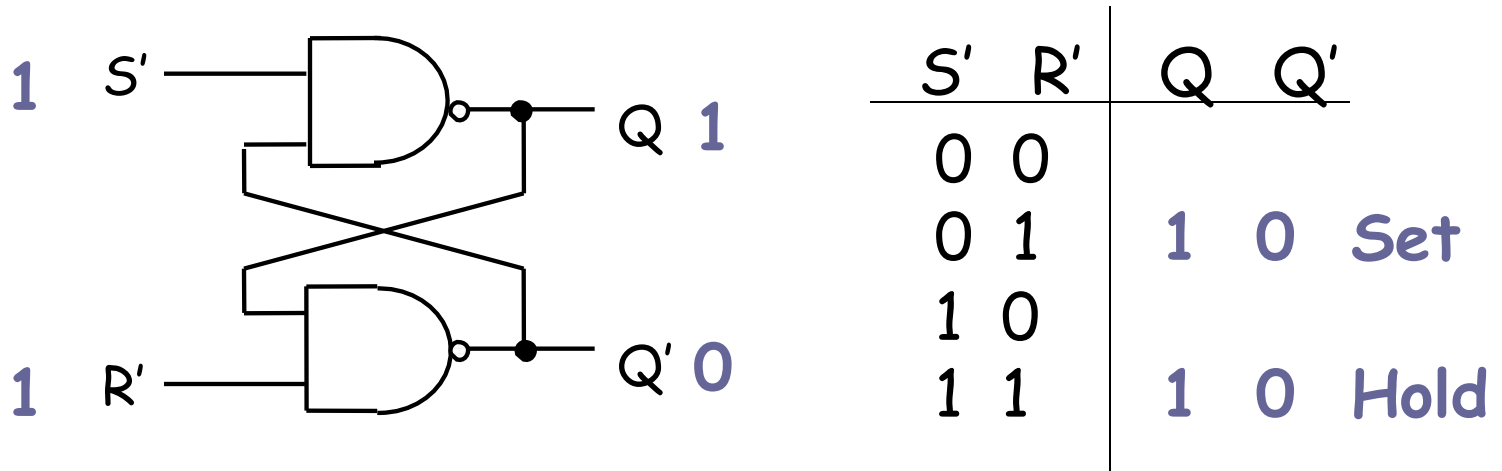
Smallest clock period = largest combinational circuit delay between any two directly connected FF, subjected to impact of FF setup time.

# SR Latch (NAND version)



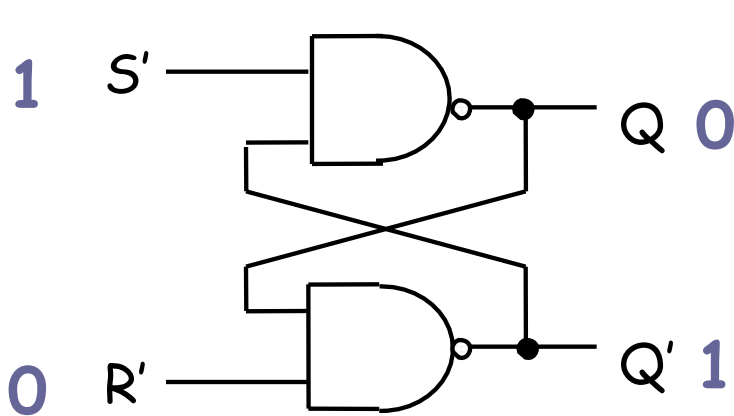
$X$	$Y$	NAND
0	0	1
0	1	1
1	0	1
1	1	0

# SR Latch (NAND version)



X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

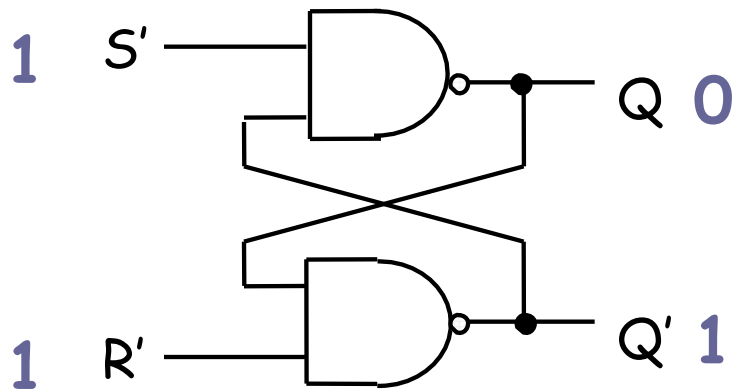
# SR Latch (NAND version)



$S'$	$R'$	$Q$	$Q'$	
0	0			
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold

$X$	$Y$	NAND
0	0	1
0	1	1
1	0	1
1	1	0

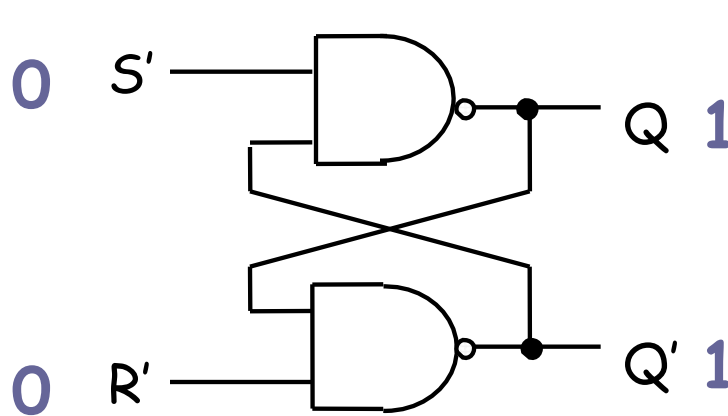
# SR Latch (NAND version)



$S'$	$R'$	$Q$	$Q'$	
0	0			
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold
		0	1	Hold

$X$	$Y$	NAND
0	0	1
0	1	1
1	0	1
1	1	0

# SR Latch (NAND version)

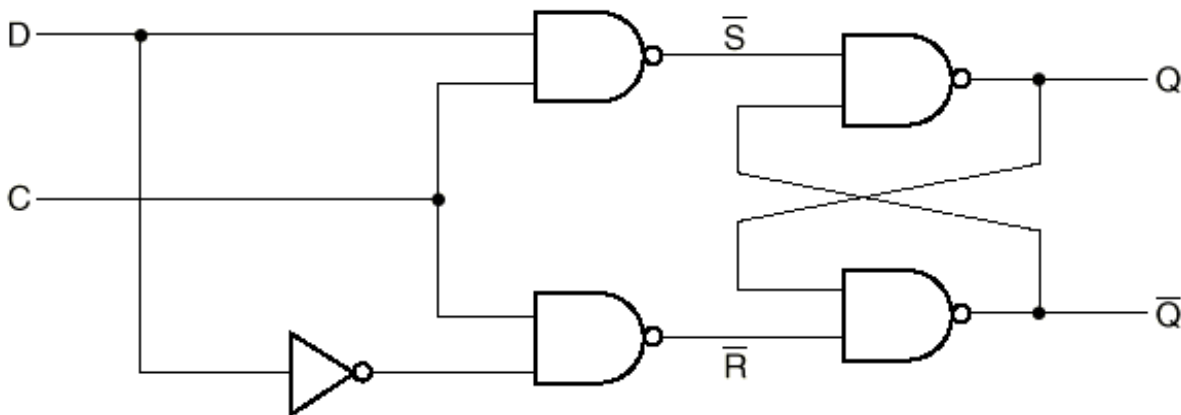


$S'$	$R'$	$Q$	$Q'$	
0	0	1	1	Disallowed
0	1	1	0	Set
1	0	0	1	Reset
1	1	1	0	Hold
		0	1	Hold

$X$	$Y$	NAND
0	0	1
0	1	1
1	0	1
1	1	0

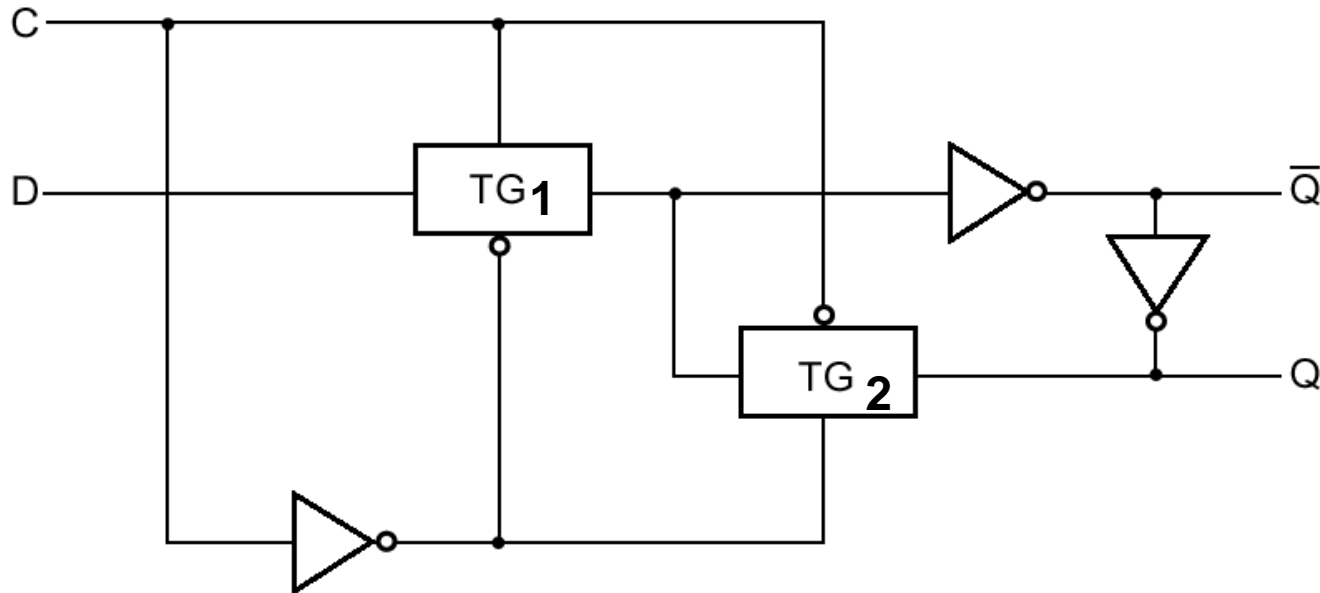
# D Latch

■ One way to eliminate the undesirable indeterminate state in the RS flip flop is to ensure that inputs S and R are never 1 simultaneously. This is done in the *D latch*:



C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

# D Latch with Transmission Gates



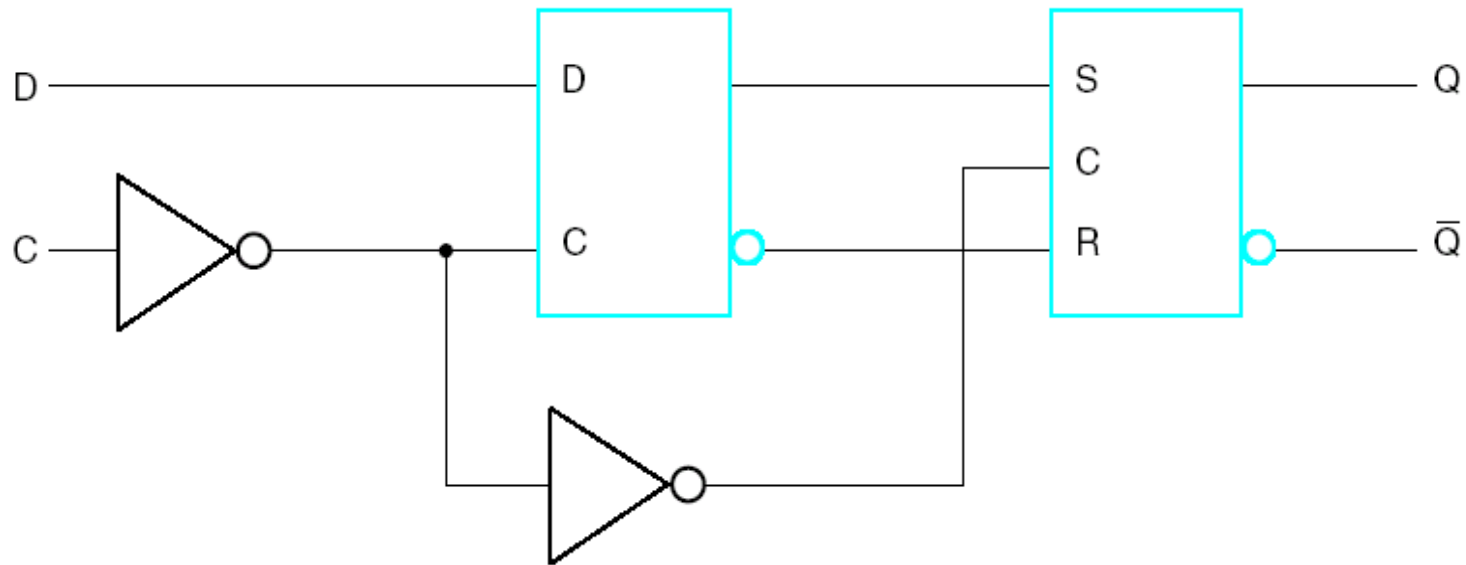
- $C=1 \rightarrow$  TG1 closes and TG2 opens  $\rightarrow Q' = D'$  and  $Q = D$
- $C=0 \rightarrow$  TG1 opens and TG2 closes  $\rightarrow$  Hold Q and  $Q'$



# Flip-Flops

- Latches are “transparent” (= any change on the inputs is seen at the outputs immediately when  $C=1$ ).
- This causes synchronization problems.
- Solution: use latches to create flip-flops that can respond (update) only on specific times (instead of any time).
- Types: RS flip-flop and D flip-flop

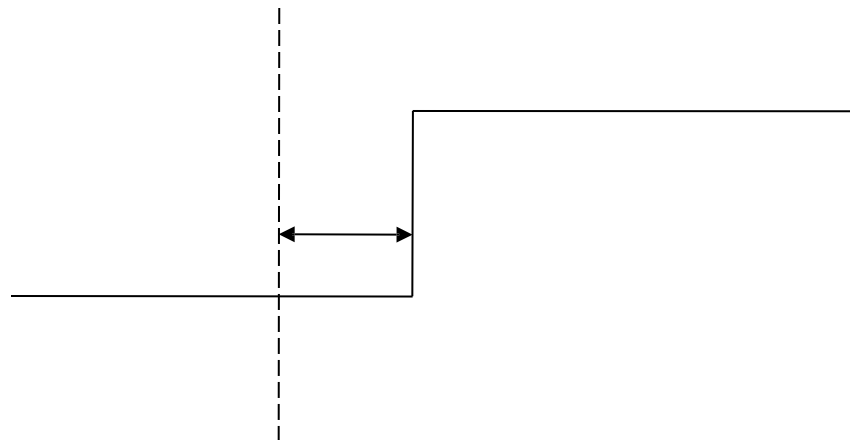
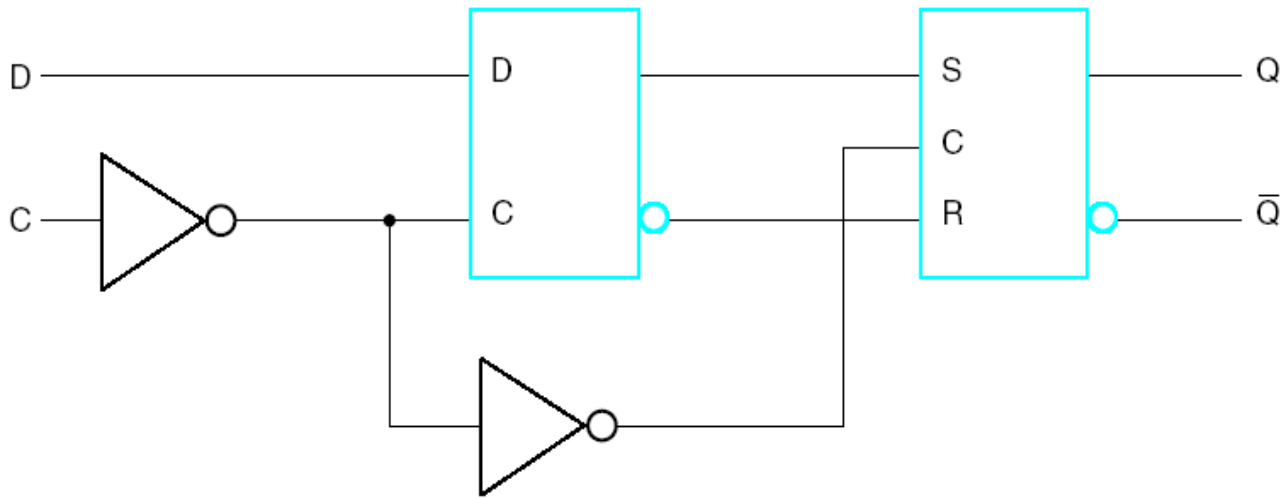
# D Flip-Flop



# Characteristic Tables

- Defines the logical properties of a flip-flop (such as a truth table does for a logic gate).
- $Q(t)$  – present state at time  $t$
- $Q(t+1)$  – next state at time  $t+1$

# D Flip-Flop Timing Parameters



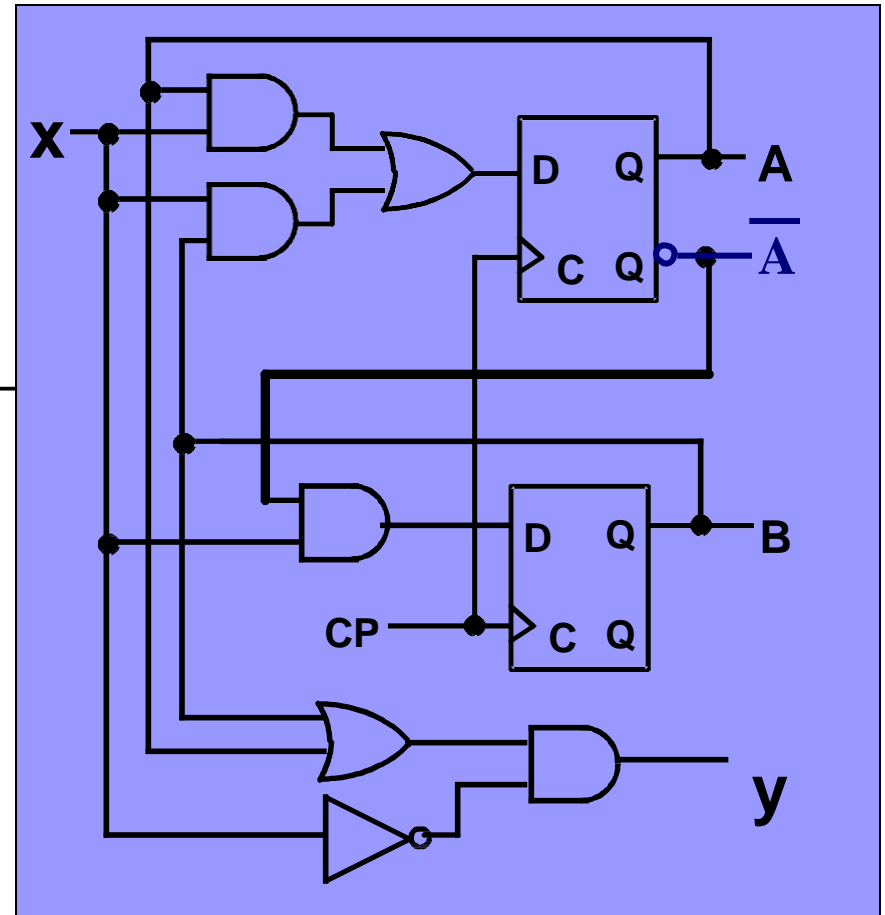
Setup time

# Sequential Circuit Analysis

- ***Analysis***: Consists of obtaining a suitable description that demonstrates the time sequence of inputs, outputs, and states.
- Logic diagram: Boolean gates, flip-flops (of any kind), and appropriate interconnections.
- The logic diagram is derived from any of the following:
  - Boolean Equations (FF-Inputs, Outputs)
  - State Table
  - State Diagram

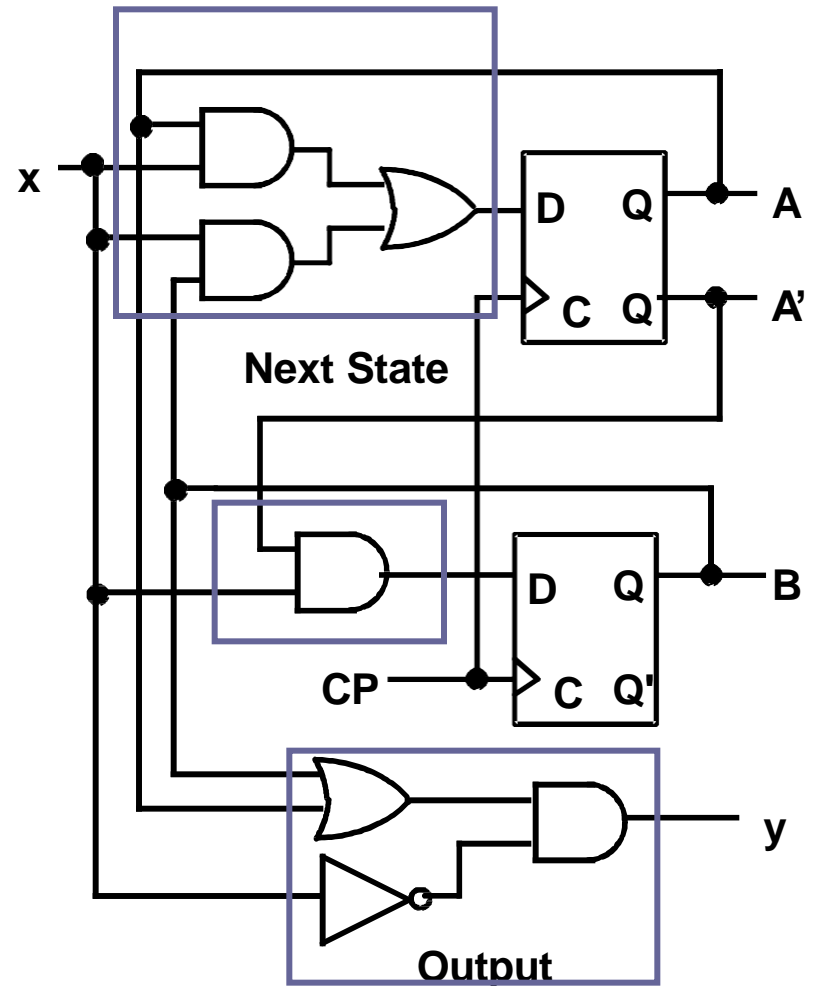
# Example

- Input:  $x(t)$
- Output:  $y(t)$
- State:  $(A(t), B(t))$
- What is the Output
- What is the Next State Function?



# Example (continued)

- Boolean equations for the functions:
  - $A(t+1) = A(t)x(t) + B(t)x(t)$
  - $B(t+1) = A'(t)x(t)$
  - $y(t) = x'(t)(B(t) + A(t))$



# State Table Characteristics

- *State table* – a multiple variable table with the following four sections:
  - *Present State* – the values of the state variables for each allowed state.
  - *Input* – the input combinations allowed.
  - *Next-state* – the value of the state at time  $(t+1)$  based on the present state and the input.
  - *Output* – the value of the output as a function of the present state and (sometimes) the input.
- From the viewpoint of a truth table:
  - the inputs are Input, Present State
  - and the outputs are Output, Next State

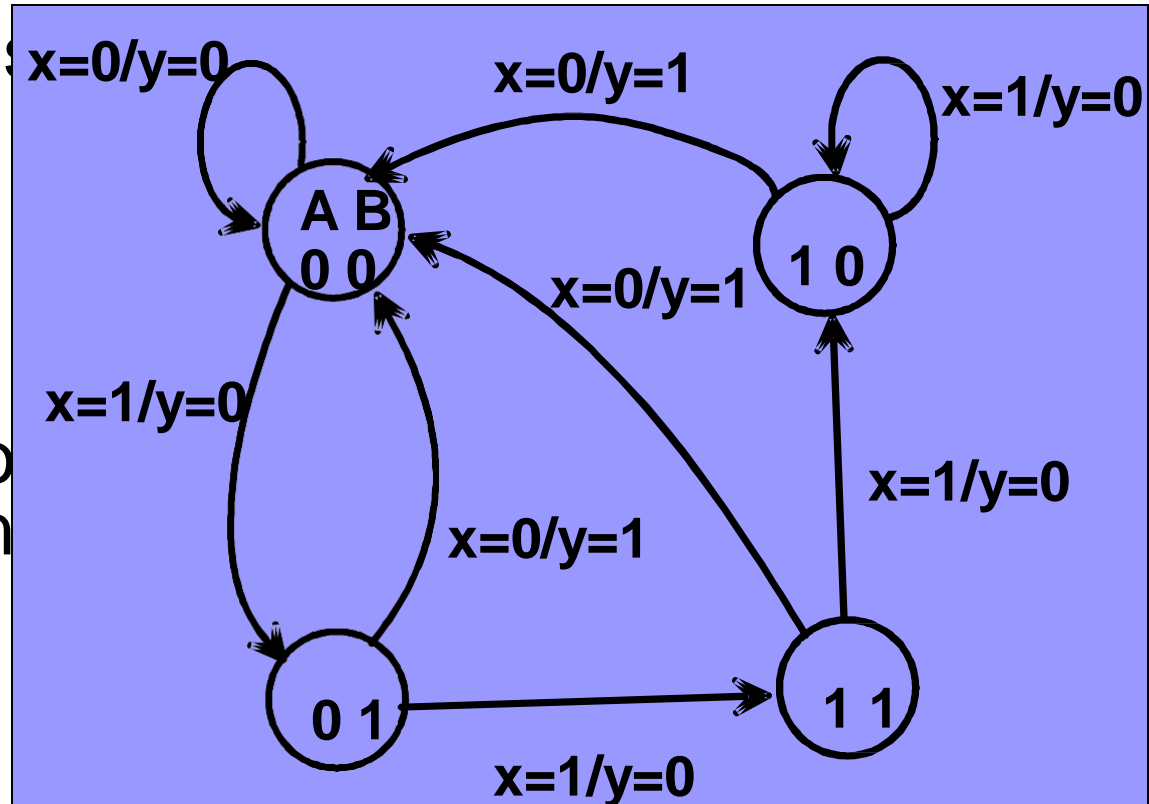


# State Diagrams

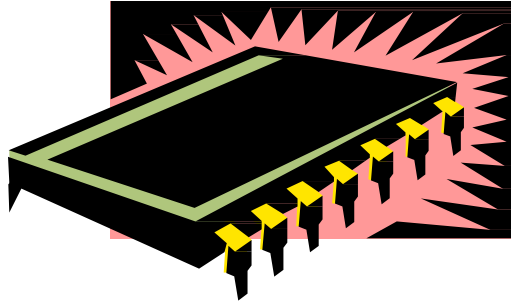
- The sequential circuit function can be represented in graphical form as a state diagram with the following components:
  - A circle with the state name in it for each state
  - A directed arc from the Present State to the Next State for each state transition
  - A label on each directed arc with the Input values which causes the state transition, and
  - A label:
    - On each circle with the output value produced, or
    - On each directed arc with the output value produced.

# Example: State Diagram

- Diagram gets confusing for large circuits
- For small circuit usually easier to understand than the state table



# MEMORY

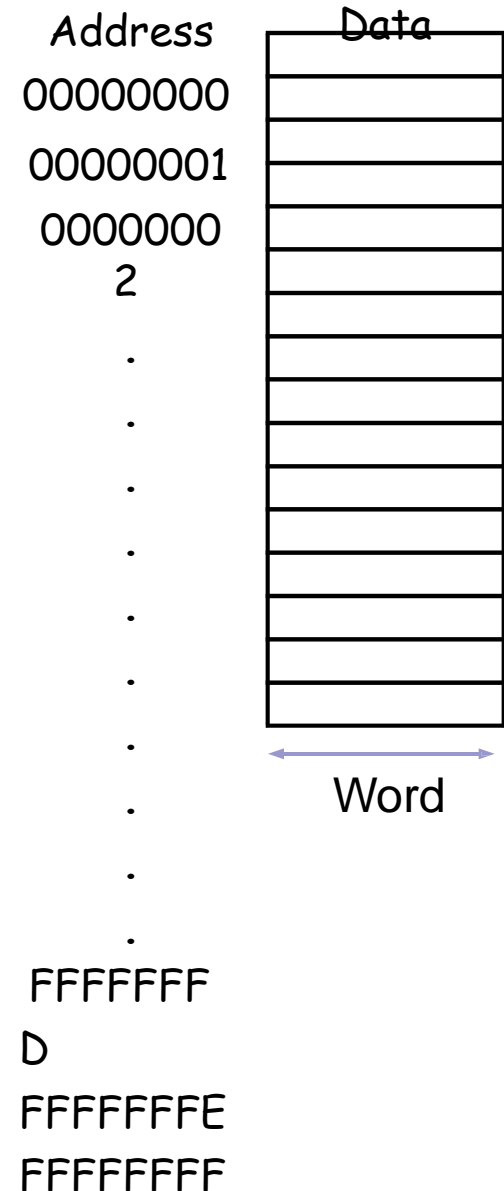


# Memory

- Sequential circuits all depend upon the presence of memory.
  - A flip-flop can store one bit of information.
  - A register can store a single “word,” typically 32 or 64 bits.
- Memory allows us to store even larger amounts of data.
  - Read Only Memory (ROM)
  - Random Access Memory (RAM)
    - Static RAM (SRAM)
    - Dynamic RAM (DRAM)

# Picture of Memory

- You can think of memory as being one big array of data.
  - The address serves as an array index.
  - Each address refers to one word of data.
- You can read or modify the data at any given memory address, just like you can read or modify the contents of an array at any given index.



# Memory Signal Types

- Memory signals fall into three groups
  - **Address bus** - selects one of memory locations
  - **Data bus**
    - **Read**: the selected location's stored data is put on the data bus
    - **Write (RAM)**: The data on the data bus is stored into the selected location
  - **Control signals** - specifies what the memory is to do
    - Control signals are usually active low
    - Most common signals are:
      - CS: Chip Select; must be active to do anything
      - OE: Output Enable; active to read data
      - WR: Write; active to write data

# Memory Address, Location and size

- All bits in location are read/written together
- Cannot manipulate single bits in a location
- For **k address signals**, there are  $2^k$  locations in memory device
- Each location contains an **n bit word**
- Memory size is specified as
  - #loc x bits per location
    - $2^{24} \times 16$  RAM -  $2^{24} = 16\text{M}$  words, each 16 bits long
    - 24 address lines, 16 data lines
  - #bits
    - The total **storage capacity** is  $2^{24} \times 16 = 2^{28}$  bits

# Size matters!

- Memory sizes are usually specified in numbers of **bytes** (1 byte= 8 bits).
- The  $2^{28}$ -bit memory on the previous page translates into:

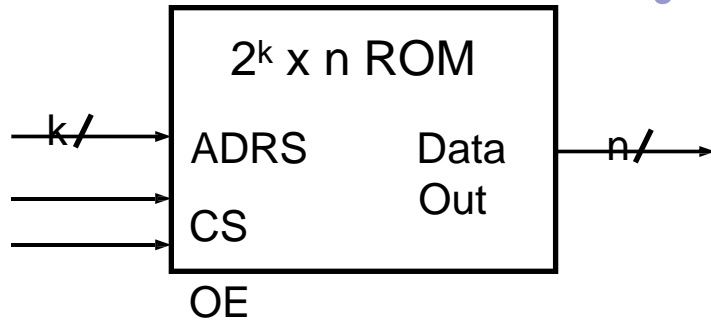
$$2^{28} \text{ bits} / 8 \text{ bits per byte} = 2^{25} \text{ bytes}$$

- With the abbreviations below, this is equivalent to 32 megabytes.

	Prefix	Base 2	Base 10
K	Kilo	$2^{10} = 1,024$	$10^3 = 1,000$
M	Mega	$2^{20} = 1,048,576$	$10^6 = 1,000,000$
G	Giga	$2^{30} = 1,073,741,824$	$10^9 = 1,000,000,000$



# Read-only memory (ROM)



- Non-volatile
    - If un-powered, its content retains
  - Read-only
    - normal operation cannot change contents
- 
- **k-bit ADRS** specifies the address or location to read from
  - A Chip Select, **CS**, enables or disables the RAM
  - An Output Enable, **OE**, turns on or off tri-state output buffers
  - **Data Out** will be the n-bit value stored at ADRS

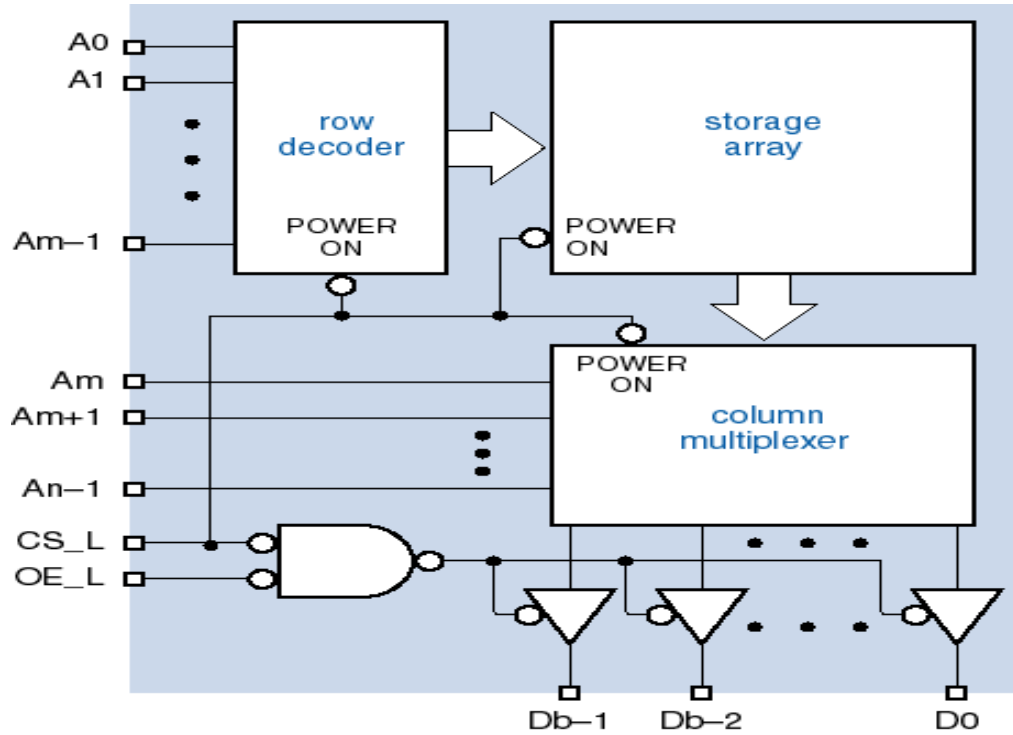
# ROM PROGRAMMING

- Programmed ROM (PROM): contents loaded at the factory
  - hardwired - can't be changed
  - embedded mass-produced systems
- OTP (One Time Programmable): Programmed by user
- UV PROM: reusable, erased by UV light
- EEPROM: Electrically erasable; clears entire blocks with single operation

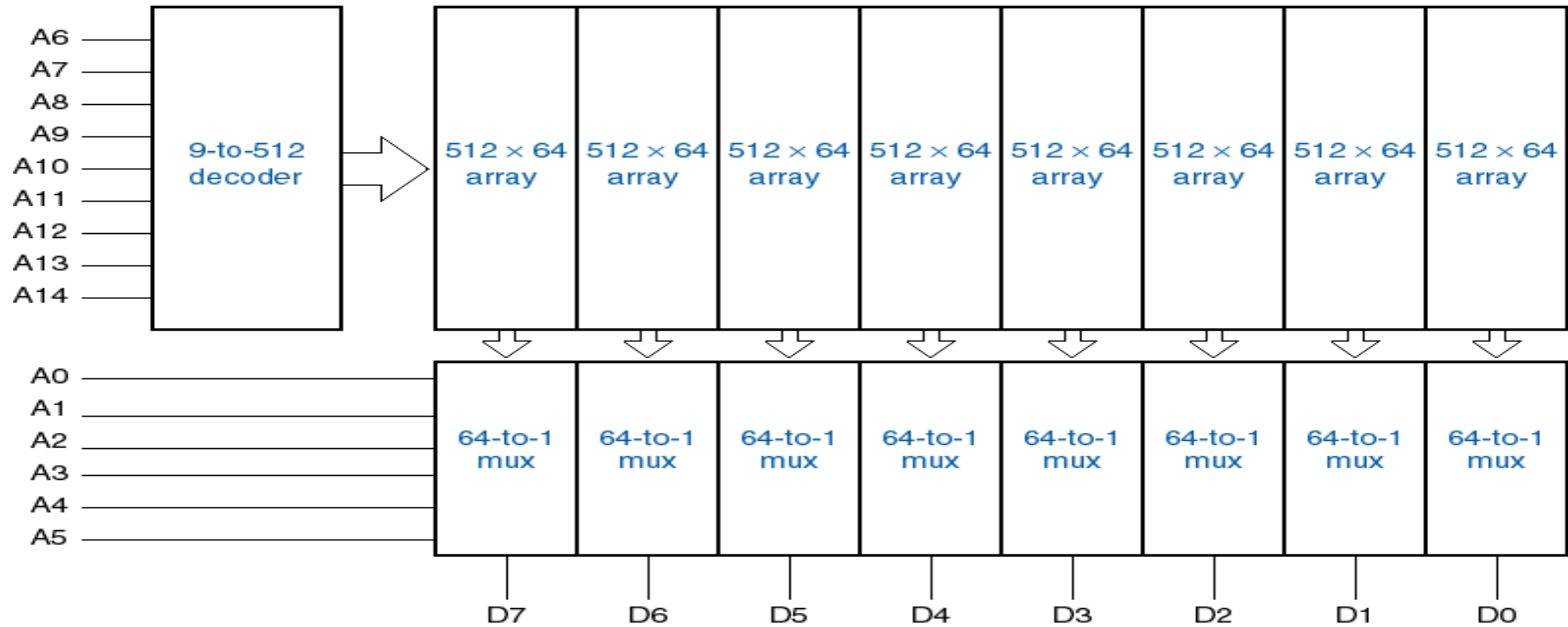
# ROM Usage

- ROMs are useful for holding data that never changes.
  - Arithmetic circuits might use tables to speed up computations of logarithms or divisions.
  - Many computers use a ROM to store important programs that should not be modified, such as the system BIOS.
  - Application programs of embedded systems, PDAs, game machines, cell phones, vending machines, etc., are stored in ROMs

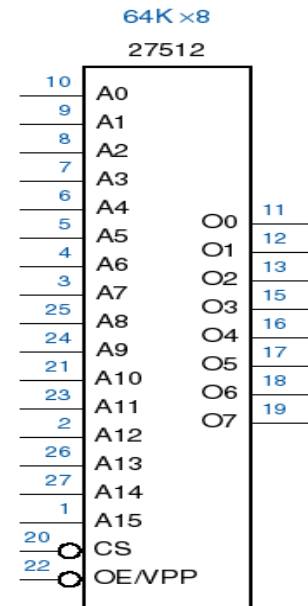
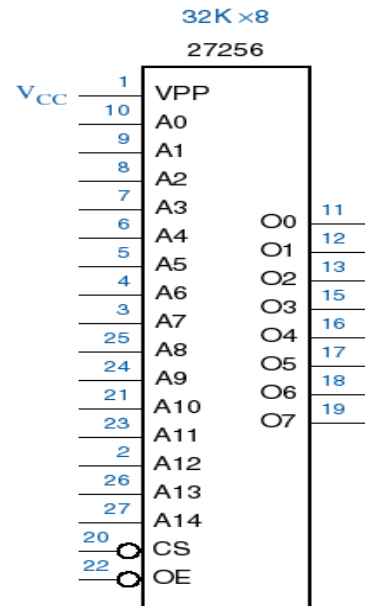
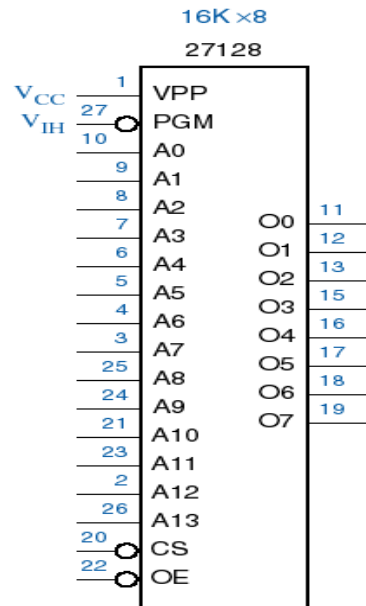
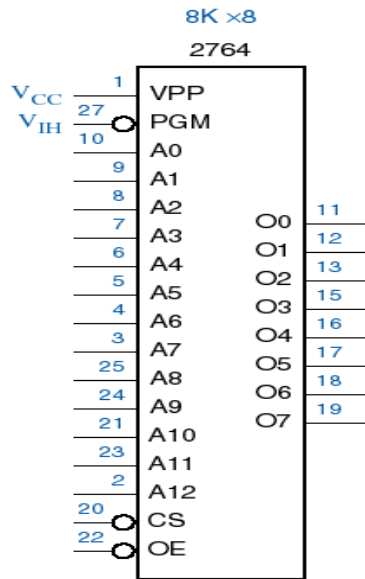
# ROM Structure



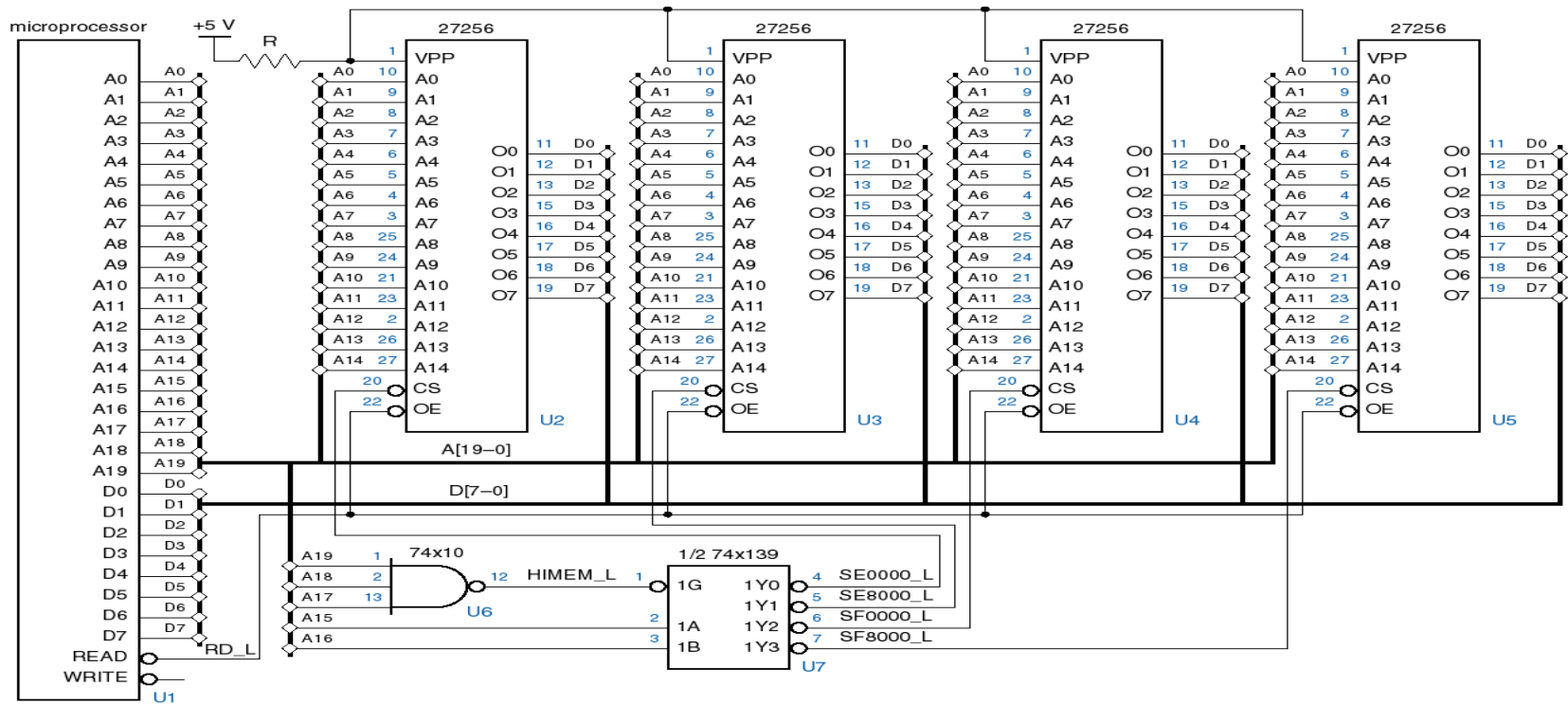
# 32Kx8 ROM



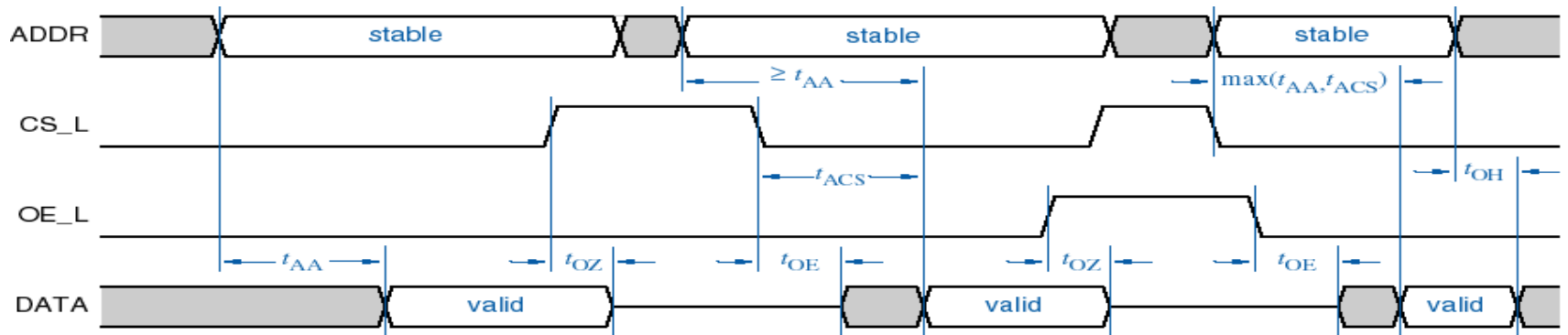
# Typical commercial EEPROMs



# Microprocessor EPROM application



# ROM Timing



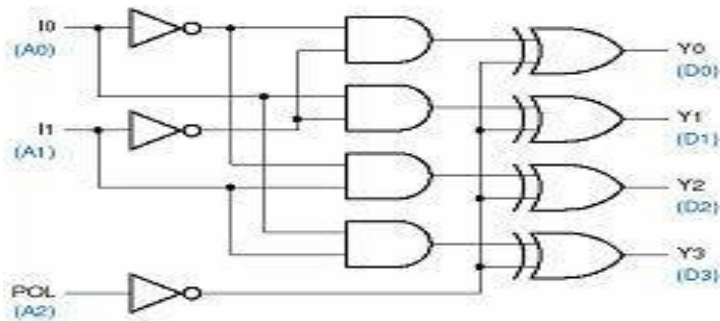


# Memories and functions

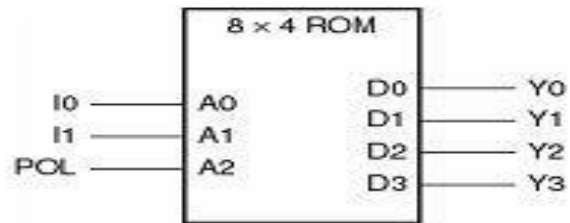
- ROMs are actually combinational devices, not sequential ones!
  - You can store arbitrary data into a ROM, so the same address will always contain the same data.
  - You can think of a ROM as a combinational circuit that takes an address as input, and produces some data as the output.
- A **ROM table** is basically just a truth table.
  - The table shows what data is stored at each ROM address.
  - You can generate that data combinatorially, using the address as the input.

Address $A_2A_1A_0$	Data $V_2V_1V_0$
000	000
001	100
010	110
011	100
100	101
101	000
110	011
111	011

# Logic-in-ROM Example

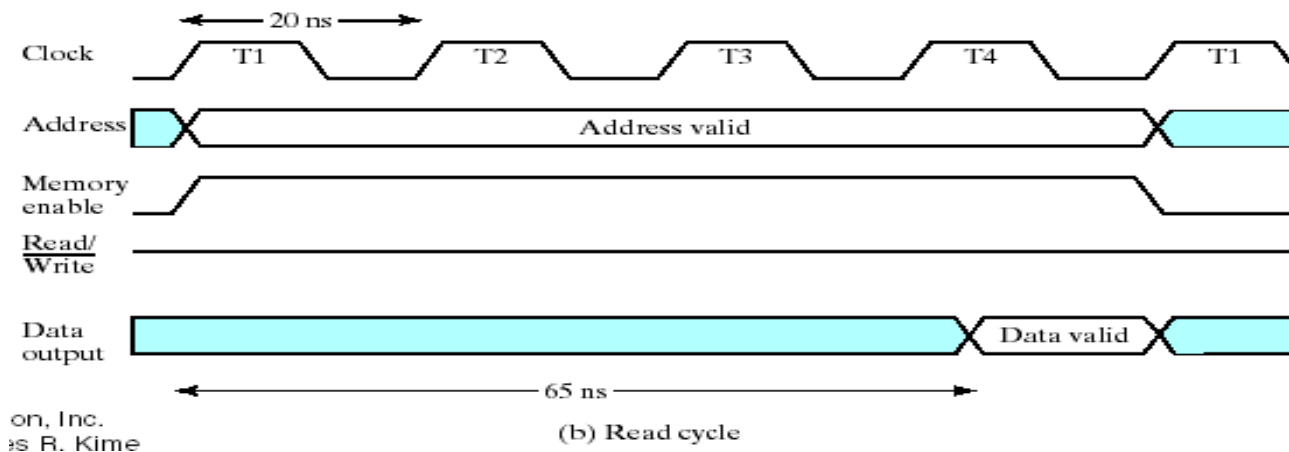


Inputs			Outputs			
A2	A1	A0	D3	D2	D1	D0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

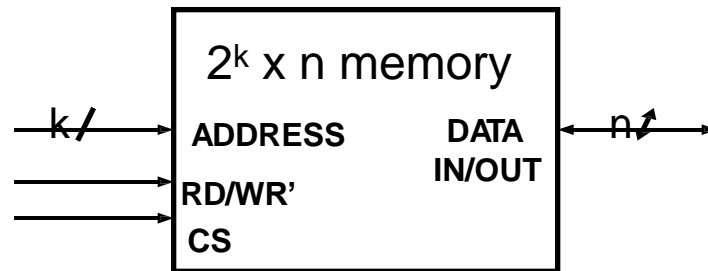


# Reading RAM

- 50 MHz CPU – 20 ns clock cycle time
- **Memory access time** = 65 ns
  - Maximum time from the application of the address to the appearance of the data at the Data Output



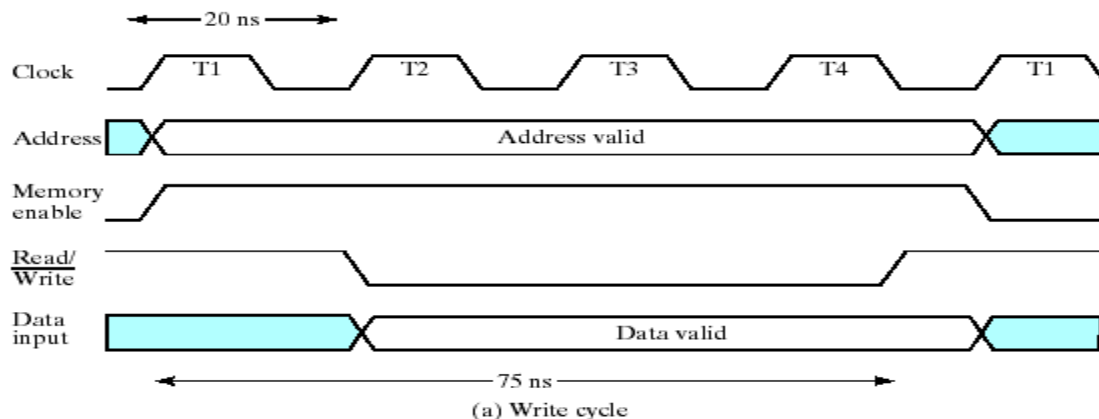
# WRITING RAM



- Enable the chip by setting  $CS = 1$ .
- Select the write operation, by setting  $RD/WR' = 0$ .
- Send the desired address to the ADDRESS input.
- Send the word to store to the DATA IN/OUT.

# WRITING RAM

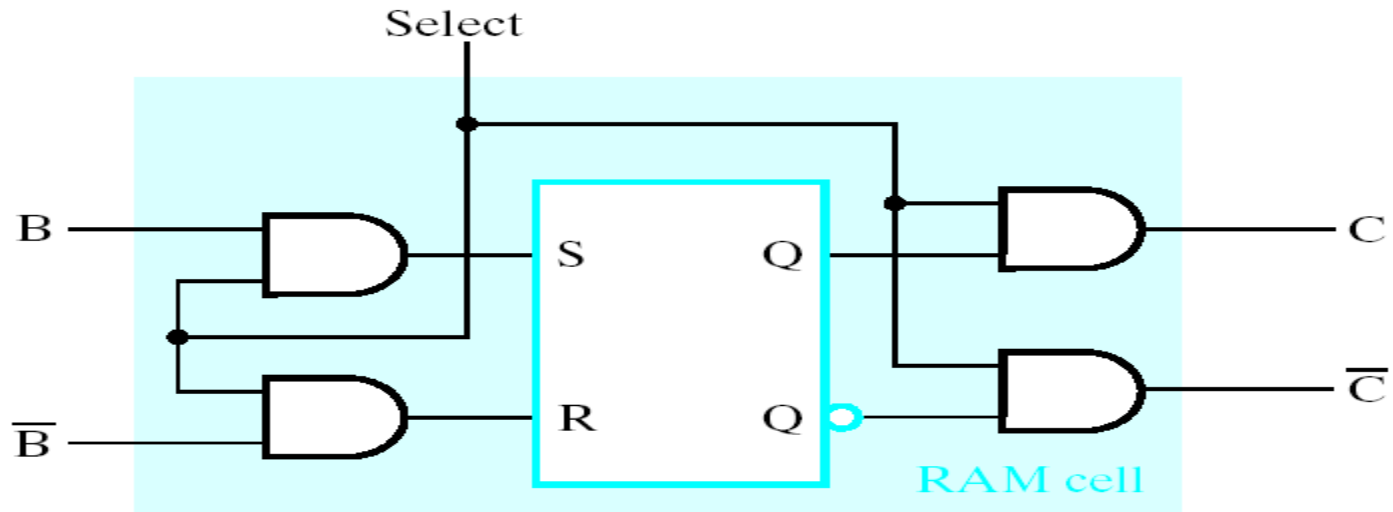
- 50 MHz CPU – 20 ns clock cycle time
- Write cycle time = 75 ns
  - Maximum time from the application of the address to the completion of all internal memory operations to store a word



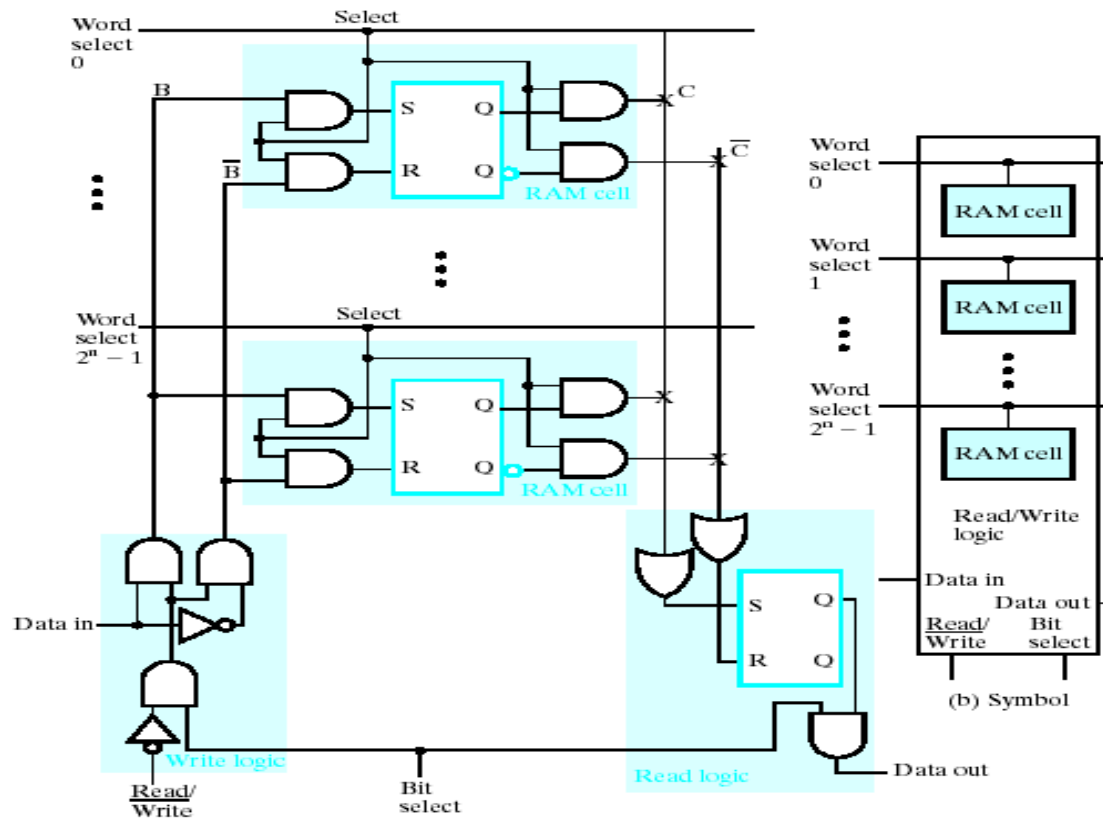
# Static memory

- How can you implement the memory chip?
- There are many different kinds of RAM.
  - We'll start off discussing **static memory**, which is most commonly used in caches and video cards.
  - Later we mention a little about **dynamic memory**, which forms the bulk of a computer's main memory.
- Static memory is modeled using one *latch* for each bit of storage.
- Why use latches instead of flip flops?
  - A latch can be made with only two NAND or two NOR gates, but a flip-flop requires at least twice that much hardware.
  - In general, smaller is faster, cheaper and requires less power.
  - The tradeoff is that getting the timing exactly right is a pain.

# RAM Cell with SR Latch

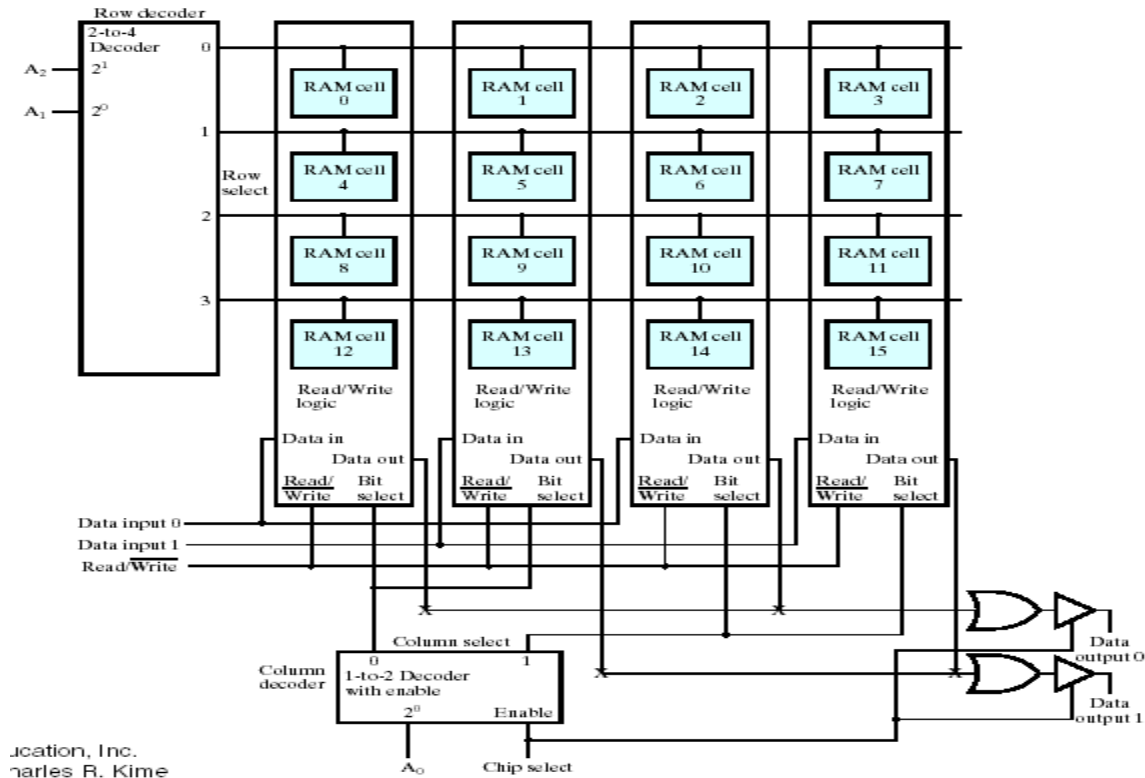


# RAM Bit Slice Model

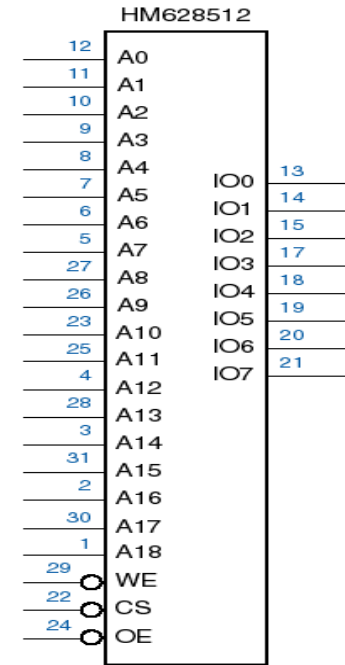
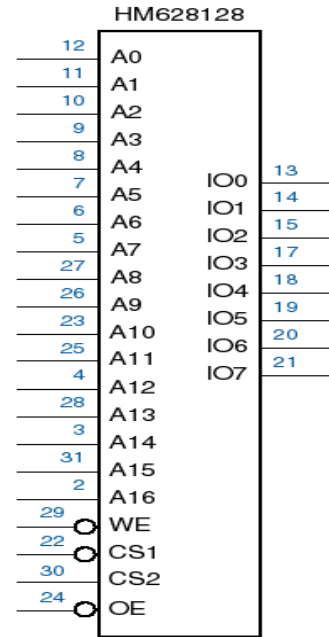
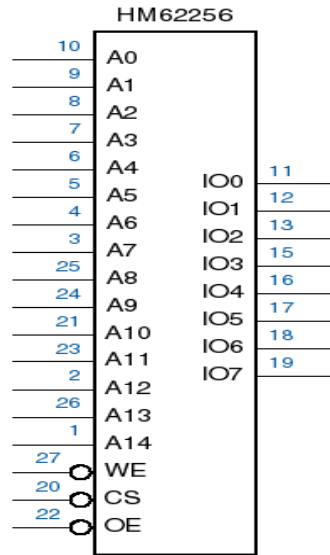
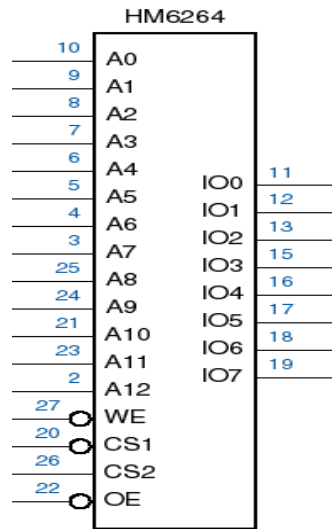




# 8x2 RAM Using a 4x4 RAM Cell Array



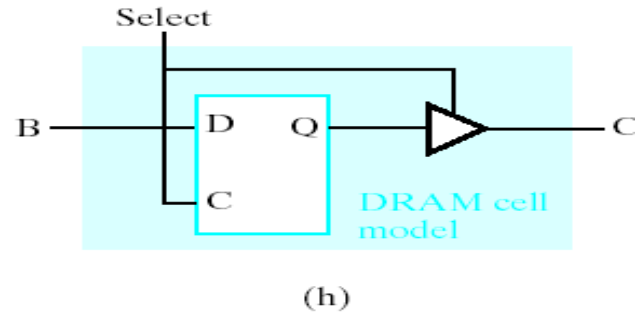
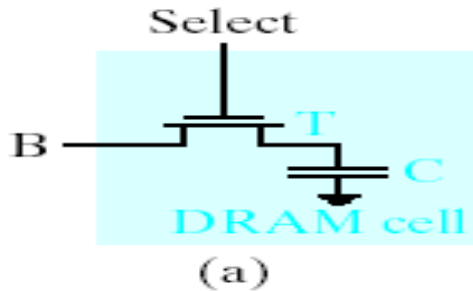
# SRAM Devices



# Dynamic memory

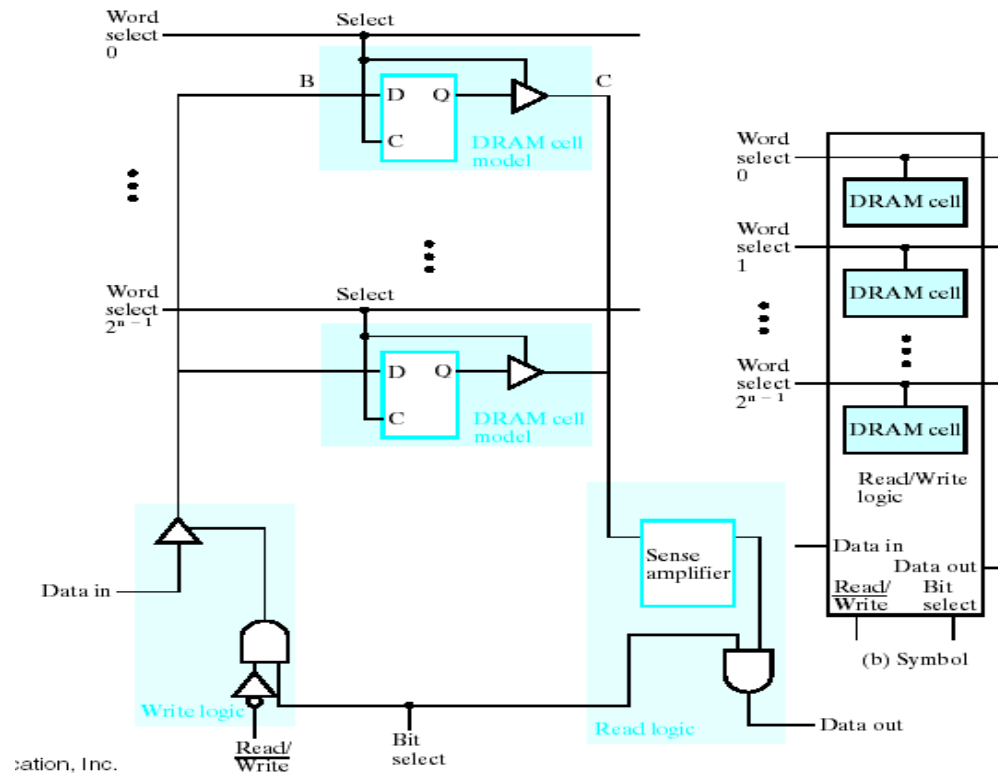
- **Dynamic memory** is built with capacitors.
  - A stored charge on the capacitor represents a logical 1.
  - No charge represents a logic 0.
- However, capacitors lose their charge after a few milliseconds. The memory requires constant **refreshing** to recharge the capacitors. (That's what's "dynamic" about it.)
- Dynamic RAMs tend to be physically smaller than static RAMs.
  - A single bit of data can be stored with just one capacitor and one transistor, while static RAM cells typically require 4-6 transistors.
  - This means dynamic RAM is cheaper and denser—more bits can be stored in the same physical area.

# DRAM Cell



- DRAM cell: One transistor and one capacitor
  - 1/0 = capacitor charged/discharged
- SRAM cell: Six transistors – Costs 3 times more (cell complexity)
- Cost per bit is less for DRAM – reason for why large memories are DRAMs

# DRAM Bit Slice



# DRAM Including Refresh Logic

