JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
Draft Academic Regulations of M.Tech. (Full Time/Regular) Programme
(Effective for the students admitted into I year from the Academic Year 2021-22 and onwards)

Jawaharlal Nehru Technological University Anantapur (JNTUA) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Jawaharlal Nehru Technological University Anantapur shall confer M. Tech. degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. **Award of the M.Tech. Degree**
   A student will be declared eligible for the award of the M.Tech. degree if he/she fulfils the following:
   1.1 Pursues a course of study for not less than two academic years and not more than four academic years.
   1.2 Registers for 70 credits and secures all 70 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

3. **Programme of Study:**
   The following M.Tech. Specializations are offered at present in different branches of Engineering and Technology in non-autonomous affiliated colleges:

S.No.	Discipline	Name of the Specialization	Code
01	Civil Engineering	Structural Engineering	20
		Geotechnical Engineering	12
		Computer Aided Structural Engineering	35
		Construction Planning &Management	21
		Structural Engineering &Construction Management	91
		Highway Engineering	93
02	Electrical and Electronics Engineering	Electrical Power Systems	07
		Power Electronics	43
		Power Electronics & Electrical Drives	54
		Power Systems	82
03	Mechanical Engineering	CAD / CAM	04
		Machine Design	15
		Thermal Science & Energy Systems	11
		Refrigeration & Air- Conditioning	17
		Advanced Manufacturing Systems	87

		Thermal Engineering	88
		Production Engineering &Engineering Design	90
		Production Engineering	94
04	Electronics and Communication Engineering	Digital Electronics & Communication Systems	38
		Electronics & Communication Engineering	70
		Digital Systems & Computer Electronics	06
		Embedded Systems	55
		VLSI Design	57
		VLSI System Design	
		VLSI	
		VLSI & Embedded Systems	68
		Embedded Systems & VLSI	
		VLSI and Embedded Systems Design	85
05	Computer Science and Engineering	Computer Science & Engineering	58
		Software Engineering	25
		Computer Networks	08
		Artificial Intelligence & Machine Learning	98

and any other specializations as approved by AICTE/University from time to time.

4. **Eligibility for Admissions**:

4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.

4.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes/an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. **Programme related terms:**

5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for students to select from the prescribed courses.

6. **Programme Pattern:**

6.1 Total duration of the of M.Tech. programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M.Tech. degree programme are broadly classified as follows:

S.No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/department/ branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Research	Research methodology & IPR	To understand importance and process of creation of patents through research
		Technical Seminar	Ensures preparedness of students to undertake major projects/Dissertation, based on core contents related to specialization
		Cocurricular Activities	Attending conferences, scientific presentations and other scholarly activities
		Dissertation	M.Tech. Project or Major Project
4.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc.

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

7.1 A student shall be eligible to appear for the University external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) each question for 10 marks. Final Internal marks for a total of 30 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other. There shall be an online examination (TWO) conducted during the respective mid examinations by the college for the remaining 10 marks with 20 objective questions.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.
ii. All the questions have to be answered compulsorily.
iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.

The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva-voce-15.

8.5 There shall be a **Technical Seminar** during I year II semester for internal evaluation of 100 marks. A student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other faculty members of the department. The student has to secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when supplementary examinations are conducted. The Technical seminar shall be conducted anytime during the semester as per the convenience of the Project Review Committee and students. There shall be no external examination for Technical Seminar.

8.6 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re-examination shall be conducted for failed candidates for 40 marks every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.7 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.8 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.9 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the University norms and shall be produced to the Committees of the University as and when the same are asked for.

9. **Credit Transfer Policy**

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the University shall allow up to a maximum of 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

9.1 The University shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester

9.7 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.8 The university shall ensure no overlap of SWAYAM MOOC exams with that of the university examination schedule. In case of delay in SWAYAM results, the university will re-issue the marks sheet for such students.

9.9 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.

9.10 The institution shall submit the following to the examination section of the university:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.11 The university shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the

light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval of the University at least three months prior to the commencement of the semester.

10. **Re-registration for Improvement of Internal Evaluation Marks**:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For reregistration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Internal evaluation of the Project Work – I & Project work – II in III & IV semesters respectively shall be for 100 marks each. External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.4 Project work shall be carried out under the supervision of teacher in the parent department concerned.

11.5 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases,one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

11.6 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.7 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.8 After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.9 The Project Work Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.10 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.

11.11 The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress

of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.

11.12 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.13 After approval from the PRC, the students are required to submit a report showing that the plagiarism is within 30%. The dissertation report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the dissertation report.

11.14 Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the dissertation.

11.15 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.16 The dissertation shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each student. However, the dissertation will be adjudicated by one examiner nominated by the University.

11.17 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University

11.18 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.19 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

11.20 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12. Credits for Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the principals of the colleges and the same shall be submitted to the University.

A Student shall earn 02 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits / Activity
Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student)	1
Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student)	2
Academic Award/Research Award from State Level/National Agencies	1
Academic Award/Research Award from International Agencies	2
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	1
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	2

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

13. Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

i) A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.
ii) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i)/ \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.
ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale.
Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

14. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	Percentage of Marks to be secured
First Class with Distinction	≥70%
First Class	< 70% ≥ 60%
Pass Class	< 60% ≥ 50%

15. **Exit Policy:** The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

    The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

16. Withholding of Results:

If the candidate has any case of in-discipline pending against him, the result of the candidate shall be withheld, and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

17. **Transitory Regulations**

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

18. General:

17.1 The academic regulations should be read as a whole for purpose of any interpretation.

17.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

17.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.

17.4 Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

17.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

17.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

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RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all University examinations if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ officer-in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project

		work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

1. Malpractices identified by squad or special invigilators
2. Punishments to the candidates as per the above guidelines.
3. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
4. A show cause notice shall be issued to the college.
5. Impose a suitable fine on the college.
6. Shifting the examination center from the college to another college for a specific period of not less than one year.

Note:

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

SEMESTER – I

S. No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D57101	CMOS Analog IC Design	PC	3	0	0	3
2.	21D57102	CMOS Digital IC Design	PC	3	0	0	3
3.	21D57103a 21D57103b 21D57103c	**Program Elective – 1** Microchip Fabrication Techniques Nanomaterials and Nanotechnology CAD for VLSI	PE	3	0	0	3
4.	21D57104a 21D57104b 21D57104c	**Program Elective – 1** Device Modelling FPGA Architectures and Applications ASIC Design	PE	3	0	0	3
5.	21D57105	CMOS Analog IC Design Lab	PC	0	0	4	2
6.	21D57106	CMOS Digital IC Design Lab	PC	0	0	4	2
7.	21DRM101	Research Methodology and IPR	MC	2	0	0	2
8.	21DAC101a 21DAC101b 21DAC101c	**Audit Course – I** English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	AC	2	0	0	0
Total							**18**

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SEMESTER – II

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D57201	CMOS Mixed Signal IC Design	PC	3	0	0	3
2.	21D57202	Physical Design Automation	PC	3	0	0	3
3.	21D57203a 21D57203b 21D57203c	**Program Elective – III** SoC Testing and Verification Semiconductor Memory Design and Testing MEMS System Design	PE	3	0	0	3
4.	21D57204a 21D57204b 21D57204c	**Program Elective – IV** Low Power VLSI Design IoT and its Applications VLSI Signal Processing	PE	3	0	0	3
5.	21D57205	CMOS Mixed Signal IC Design Lab	PC	0	0	4	2
6.	21D57206	Physical Design Automation Lab	PC	0	0	4	2
7.	21D57207	Technical seminar	PR	0	0	4	2
8.	21DAC201a 21DAC201b 21DAC201c	**Audit Course – II** Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	AC	2	0	0	0
		Total					**18**

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COMMON COURSE STRUCTURE & SYLLABI

SEMSTER - III

S.No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D57301a 21D57301b 21D06203a	**Program Elective – V** Bi-CMOS Technology and Applications Optimization Techniques and Applications in VLSI Design SoC Architecture	PE	3	0	0	3
2.	21DOE301b 21DOE301c 21DOE301e	**Open Elective** Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3
3.	21D57302	Dissertation Phase – I	PR	0	0	20	10
4.	21D57303	Co-curricular Activities					2
Total							**18**

SEMESTER - IV

S.No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D57401	Dissertation Phase – II	PR	0	0	32	16
Total							**16**

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS ANALOG IC DESIGN	L	T	P	C
21D57101		3	0	0	3
	Semester	I			

Course Objectives:

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes (CO): Student will be able to

- Design MOSFET based analog integrated circuits.
- Analyze analog circuits at least to the first order.
- Appreciate the trade-offs involved in analog integrated circuit design.
- Understand and appreciate the importance of noise and distortion in analog circuits.
- Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area

UNIT - I Lecture Hrs:

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT - II Lecture Hrs:

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit

UNIT - III Lecture Hrs:

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT - IV Lecture Hrs:

Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT - V Lecture Hrs:

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks:

1. B.Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd Edition, McGraw Hill Edition2016.
2. Paul.R.Gray& Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley,

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COMMON COURSE STRUCTURE & SYLLABI

5thEdition, 2009.
Reference Books:
1.T.C.Carusone, D.A.Johns&K.Martin, "Analog Integrated Circuit Design", 2ndEdition, Wiley, 2012. 2. P.E.Allen&D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011. 3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rdEdition, Wiley, 2010. 4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6thEdition, Oxford University Press

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN	L	T	P	C
21D57102		3	0	0	3
Semester		I			

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT - I		Lecture Hrs:

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II		Lecture Hrs:

Combinational MOS Logic Circuits:MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III		Lecture Hrs:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT - IV		Lecture Hrs:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V		Lecture Hrs:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

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COMMON COURSE STRUCTURE & SYLLABI

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	MICROCHIP FABRICATION TECHNIQUES	L	T	P	C
21D57103a		3	0	0	3
	Semester	**I**			

Course Objectives:

- Comprehend impact of semiconductor industry on the design of development of integrated circuits.
- Acquaint with clean room technology
- Understand oxidation methods, aspects of photolithography, diffusion, ion implantation techniques.
- Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and 45nm technologies
- Understand packaging principles

Course Outcomes (CO): Student will be able to

- Understand various stages of fabrication
- Understand Various packaging techniques and Design rules.
- Classify various thin films and its characteristics.

UNIT - I	Lecture Hrs:

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT - II	Lecture Hrs:

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT - III	Lecture Hrs:

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT - IV	Lecture Hrs:

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT - V	Lecture Hrs:

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.
Packaging: Chip characteristics, package functions, package operations.

Textbooks:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

Reference Books

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	NANOMATERIALS AND NANOTECHNOLOGY	L	T	P	C
21D57103b		3	0	0	3
	Semester	I			

Course Objectives:

- To understand the basic idea behind the design and fabrication of nano scale systems.
- To understand and frmulate new engineering solutions for current problems and technologies for future applications.
- To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

Course Outcomes (CO): Student will be able to

- Understand the basic science behind the design and fabrication of nano scale systems.
- Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
- Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
- Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

UNIT - I — Lecture Hrs:

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT - II — Lecture Hrs:

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials.Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

UNIT - III — Lecture Hrs:

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT - IV — Lecture Hrs:

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs.

UNIT - V — Lecture Hrs:

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application.

Textbooks:

1. Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2ndedition, John Wiley and Sons, 2009.
2. I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.

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3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGrawHill Education 2012.

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CAD FOR VLSI	L	T	P	C
21D57103c		3	0	0	3
	Semester	I			

Course Objectives:

- To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies
- To optimize the implemented design for area, timing and power by applying suitable constraints.

Course Outcomes (CO): Student will be able to

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- Practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT - I	Lecture Hrs:

Introduction :VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT - II	Lecture Hrs:

Partitioning : Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT - III	Lecture Hrs:

Floor Planning : Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT - IV	Lecture Hrs:

Placement and Routing : Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.
Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT - V	Lecture Hrs:

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Textbooks:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

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COMMON COURSE STRUCTURE & SYLLABI

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	DEVICE MODELLING	L	T	P	C
21D57104a		3	0	0	3
	Semester	**I**			

Course Objectives:

- To understand the physics of 2-terminal MOS operation and its characteristics
- To understand the physics of 4-terminal MOSFET operation and its characteristics.
- To analyze the SOI MOSFET electrical characteristics.

Course Outcomes (CO): Student will be able to

- Understand the physics of 2-terminal MOS operation and its characteristics
- Understand the physics of 4-terminal MOSFET operation and its characteristics.
- Analyze the SOI MOSFET electrical characteristics.

UNIT - I	Lecture Hrs:

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT - II	Lecture Hrs:

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT - III	Lecture Hrs:

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT - IV	Lecture Hrs:

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT - V	Lecture Hrs:

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Textbooks:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

Reference Books

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	FPGA ARCHITECTURES AND APPLICATIONS	L	T	P	C
21D57104b		3	0	0	3
	Semester	I			

Course Objectives:

- To acquire knowledge about various architectures and device technologies of PLD's.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and Sequential Circuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications.

Course Outcomes (CO): Student will be able to

- Acquire knowledge about various architectures and device technologies of PLD's.
- Comprehend FPGA Architectures.
- Analyze System level Design and their application for Combinational and Sequential Circuits.
- Familiarize with Anti-Fuse Programmed FPGAs.
- Apply knowledge of this subject for various design applications.

UNIT - I		Lecture Hrs:

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT - II	Field Programmable Gate Arrays	Lecture Hrs:

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT - III		Lecture Hrs:

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT - IV		Lecture Hrs:

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT - V		Lecture Hrs:

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Textbooks:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	ASIC DESIGN	L	T	P	C
21D57104c		3	0	0	3
	Semester	I			

Course Objectives:

- To understand different types of ASICs and their libraries.
- To understand about programmable ASICs, I/O modules and their interconnects.
- To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

Course Outcomes (CO): Student will be able to

- Understand different types of ASICs and their libraries.
- Understand about programmable ASICs, I/O modules and their interconnects.
- Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT - I		Lecture Hrs:

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT - II		Lecture Hrs:

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT - III		Lecture Hrs:

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT - IV		Lecture Hrs:

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT - V		Lecture Hrs:

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

Textbooks:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

Reference Books:

1. HimanshuBhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS ANALOG IC DESIGN LAB	L	T	P	C
21D57105		0	0	4	2
	Semester	I			

Course Objectives:

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- To explain the Physical Verification in Layout Design
- To fully appreciate the design and analyze of analog and mixed signal simulation
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Course Outcomes (CO):

- Explain the VLSI Design Methodologies using VLSI design tool.
- Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- Explain the Physical Verification in Layout Design
- Fully appreciate the design and analyze of analog and mixed signal simulation
- Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments:

- The students are required to design and implement any **TEN** Experiments using CMOS 130nm Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:
Software:
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator
Hardware:
Personal Computer with necessary peripherals, configuration and operating System.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN LAB	L	T	P	C
21D57106		0	0	4	2
	Semester	I			

Course Objectives:

- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO):

- Explain the VLSI Design Methodologies using any VLSI design tool.
- Grasp the significance of various design logic Circuits in full-custom IC Design.
- Explain the Physical Verification in Layout Extraction.
- Fully appreciate the design and analyze of CMOS Digital Circuits.

Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	RESEARCH METHODOLOGY AND IPR	L	T	P	C
21DRM101		2	0	0	2
	Semester	I			

Course Objectives:

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

Course Outcomes (CO): Student will be able to

- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III Lecture Hrs:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV Lecture Hrs:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT - V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.

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6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS MIXED SIGNAL IC DESIGN	L	T	P	C
21D57201		3	0	0	3
	Semester	II			

Course Objectives:

- To demonstrate first order filter with least interference
- To extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- To design different A/D, D/A, modulators, demodulators and different filter for real time applications

Course Outcomes (CO): Student will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT - I	Lecture Hrs:

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT – II	Lecture Hrs:

Phased Lock Loop (PLL) : Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs- Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III	Lecture Hrs:

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT - IV	Lecture Hrs:

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D coverters, Time- interleaved converters.

UNIT - V	Lecture Hrs:

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A

Textbooks:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2.Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PHYSICAL DESIGN AUTOMATION	L	T	P	C
21D57202		3	0	0	3
	Semester	II			

Course Objectives:

- To understand relation between automation algorithms and constraints posed by VLSI technology.
- To adopt algorithms to meet critical design parameters.
- To design area efficient logics by employing different routing algorithms and shape functions.
- To simulate and synthesis different combinational and sequential logics.

Course Outcomes (CO): Student will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions.
- Simulate and synthesis different combinational and sequential logics.

UNIT - I		Lecture Hrs:

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II		Lecture Hrs:

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT - III		Lecture Hrs:

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV		Lecture Hrs:

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

UNIT - V		Lecture Hrs:

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

Textbooks:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

Reference Books:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SoC TESTING AND VERIFICATION	L	T	P	C
21D57203a		3	0	0	3
	Semester	II			

Course Objectives:

- To understand the concepts of faults and testing in SoC
- To implement the faults using simulation tools
- To analyze BIST systems

Course Outcomes (CO): Student will be able to

- Understand the concepts of faults and testing in SoC
- Implement the faults using simulation tools
- Analyze BIST systems

UNIT - I	Lecture Hrs:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II	Lecture Hrs:

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT - III	Lecture Hrs:

Testability Measures: SCOAP Controllability and Observablity, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV	Lecture Hrs:

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V	Lecture Hrs:

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.

Reference Books:

1. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SEMICONDUCTOR MEMORY DESIGN AND TESTING	L	T	P	C
21D57203b		3	0	0	3
	Semester	II			

Course Objectives:

- To understand different types of memories, their architectural and different packing techniques of memories.
- To build fault models for memory testing.
- To analyze different parameters that lead malfunctioning of memories.
- To design reliable memories with efficient architecture to improve processes times and power.

Course Outcomes (CO): Student will be able to

- Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
- Build fault models for memory testing.
- Analyze different parameters that lead malfunctioning of memories.
- Design reliable memories with efficient architecture to improve processes times and power.

UNIT - I Lecture Hrs:

Random Access Memory Technologies :SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT - II Lecture Hrs:

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT - III Lecture Hrs:

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance :
RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT - IV Lecture Hrs:

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT - V Lecture Hrs:

Advanced Memory Technologies and High-density Memory Packing Technologies
Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Packaging Future Directions.
Textbooks:
1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley. 2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.
Reference Books:
1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, First Edition. Prentice all.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	MEMS SYSTEM DESIGN	L	T	P	C
21D57203c		3	0	0	3
	Semester	II			

Course Objectives:

- To understand the basic concepts of MEMS technology and working of MEMS devices.
- To understand and select different materials for current MEMS devices and competing technologies for future applications.
- To understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
- To analyze the various fabrication techniques in the manufacturing of MEMS Devices.

Course Outcomes (CO): Student will be able to

- Understand the basic concepts of MEMS technology and working of MEMS devices.
- Understand and select different materials for current MEMS devices and competing technologies for future applications.
- Understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
- Analyze the various fabrication techniques in the manufacturing of MEMS Devices.

UNIT - I	Lecture Hrs:

Introduction to MEMS: Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag, pressure sensors).MEMS Sensors in Internet of Things (IoT), Bio-Medical Applications

UNIT - II	Lecture Hrs:

MEMS Materials and Their Properties: Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson's ratio, density, piezo-resistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT - III	Lecture Hrs:

MEMS Fab Processes – 1: Understanding MEMS Processes & Process parameters for: Cleaning, Growth &Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT - IV	Lecture Hrs:

MEMS Fab Processes – 2: Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micromachining, Die, Wire& Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications.

UNIT - V	Lecture Hrs:

MEMS Devices: Architecture, working and basic quantitative behaviour of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices.

Textbooks:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Edition by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

Reference Books:

1.Analysis and Design Principles of MEMS Devices –Minhang Bao; Publisher: Elsevier Science.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

2. Fundamentals of Micro fabrication - by M. Madou; Publisher:CRC Press; 2ndedition
3.Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press
4.Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	LOW POWER VLSI DESIGN	L	T	P	C
21D57204a		3	0	0	3
	Semester	**II**			

Course Objectives:

- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- To implement Low power design approaches for system level and circuit level measures.
- To design low power adders, multipliers and memories for efficient design of systems.

Course Outcomes (CO): Student will be able to

- Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

UNIT - I — Lecture Hrs:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II — Lecture Hrs:

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT - III — Lecture Hrs:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV — Lecture Hrs:

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V — Lecture Hrs:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1.CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2.Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	IOT AND ITS APPLICATIONS	L	T	P	C
21D57204b		3	0	0	3
	Semester	II			

Course Objectives:

- To apply the Knowledge in IOT Technologies and Data management.
- To determine the values chains Perspective of M2M to IOT.
- To implement the state of the Architecture of an IOT.
- To compare IOT Applications in Industrial & real world.
- To demonstrate knowledge and understand the security and ethical issues of an IOT.

Course Outcomes (CO): Student will be able to

- Apply the Knowledge in IOT Technologies and Data management.
- Determine the values chains Perspective of M2M to IOT.
- Implement the state of the Architecture of an IOT.
- Compare IOT Applications in Industrial & real world.
- Demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT - I		Lecture Hrs:

Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.
IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT - II		Lecture Hrs:

IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT - III		Lecture Hrs:

Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT - IV		Lecture Hrs:

Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT - V		Lecture Hrs:

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	VLSI SIGNAL PROCESSING	L	T	P	C
21D57204c		3	0	0	3
	Semester	**II**			

Course Objectives:

- To study the existing architectures suitable for VLSI.
- To understand the concepts of folding and unfolding algorithms and applications.
- To design new architectures suitable for VLSI.
- To implement fast convolution algorithms.

Course Outcomes (CO): Student will be able to

- Study the existing architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Design new architectures suitable for VLSI.
- Implement fast convolution algorithms.

UNIT - I	Lecture Hrs:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT - II	Lecture Hrs:

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT - III	Lecture Hrs:

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT - IV	Lecture Hrs:

Fast Convolution: Introduction – Cook - Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT - V	Lecture Hrs:

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Textbooks:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998.
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985.

Reference Books

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994.
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS MIXED SIGNAL IC DESIGN LAB	L	T	P	C
21D57205		0	0	4	2
	Semester	II			

Course Objectives:

- To design and simulate op-amp for given specifications
- To design and simulate data converter for given specifications
- To design and simulate PLL and VCO for given specifications
- To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes (CO):

- Design and simulate op-amp for given specifications
- Design and simulate data converter for given specifications
- Design and simulate PLL and VCO for given specifications
- Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of the following Experiments using CMOS 130nm Technology.

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing, Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PHYSICAL DESIGN AUTOMATION LAB	L	T	P	C
21D57206		0	0	4	2
	Semester	II			

Course Objectives:

- To learn the implementation of different Physical Design Automation algorithms
- To implement different graph algorithms
- To implement different partitioning algorithms
- To implement different floor planning algorithms
- To implement different routing algorithms

Course Outcomes (CO):

- Learn the implementation of different Physical Design Automation algorithms
- Implement different graph algorithms
- Implement different partitioning algorithms
- Implement different floor planning algorithms
- Implement different routing algorithms

List of Experiments:

Cycle 1:

1) Graph algorithms
   a) Graph search algorithms
      i. Depth first search
      ii. Breadth first search
   b) Spanning tree algorithm
      i. Kruskal‟s algorithm
   c) Shortest path algorithm
      i. Dijkstra algorithm
      ii. Floyd- Warshall algorithm
   d) Steiner tree algorithm
2) Computational geometry algorithm
   a) Line sweep method
   b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
   a) Group migration algorithms
      I. Kernighan –Lin algorithm
      II. Extensions of Kernighan-Lin algorithm
         i) Fiduccias –Mattheyses algorithm
         ii) Goldberg and Burstein algorithm
   b) Simulated annealing and evolution algorithms
      i. Simulated annealing algorithm
      ii. Simulated evolution algorithm
   III) Metric allocation method

4) Floor planning algorithms
      i) Constraint based methods
      ii) Integer programming based methods
      iii) Rectangular dualization based methods
      iv) Hierarchical tree based methods

v) Simulated evolution algorithms
vi) Time driven Floor planning algorithms

5) Routing algorithms
I) Two terminal algorithms
a) Maze routing algorithms
i)Lee‟s algorithm
ii) Soukup‟s algorithm
iii) Hadlock algorithm
b) Line-Probe algorithm
c) Shortest path based algorithm
II) Multi terminal algorithm
a) Stenier tree based algorithm
i) SMST algorithm
ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Text Books:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	BICMOS TECHNOLOGY AND APPLICATIONS	L	T	P	C
21D57301a		3	0	0	3
	Semester	III			

Course Objectives:

- To demonstrate in-depth knowledge in BiCMOS Technology.
- To analyze complex engineering problems critically for conducting research in BiCMOS Technology.
- To solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- To realize different digital circuits using BiCMOS Technology

Course Outcomes (CO): Student will be able to

- Demonstrate in-depth knowledge in BiCMOS Technology.
- Analyze complex engineering problems critically for conducting research in BiCMOS Technology.
- Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- Realize different digital circuits using BiCMOS Technology

UNIT - I Lecture Hrs:

BiCMOS Process Technology: CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS and Bipolar Technologies, BiCMOS Technology, BiCMOS Design Rules.

UNIT - II Lecture Hrs:

Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations.
BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT - III Lecture Hrs:

Device Modeling: Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICE Models of the MOS Transistor,Analytical Model for Short-Channel MOS Devices.
Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-Moll Model, Bipolar Models in SPICE.

UNIT - IV Lecture Hrs:

BiCMOS DigitalIntegrated Circuits: BiMOS Totem-Pole Inveter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates.

UNIT - V Lecture Hrs:

BiCMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

Textbooks:

1.Sherif H.K. Embabi, AbdellatifBellaouar& Mohamed I. Elmasry "Digital BiCMOS Integrated Circuit Design" Springer Science+ BusÎness Media, LLC.
2.A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.

Reference Books:

1.Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2.James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press
3.KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	OPTIMIZATION TECHNIQUES AND APPLICATIONS IN VLSI DESIGN	L	T	P	C
21D57301b		3	0	0	3
	Semester	III			

Course Objectives:

- To understand basics of statistical modeling
- To analyze performance of CMOS circuits with respect to power, area and speed
- To acquire complete knowledge regarding the various algorithms used for optimization of power and area

Course Outcomes (CO): Student will be able to

- Understand basics of statistical modeling
- Analyze performance of CMOS circuits with respect to power, area and speed
- Acquire complete knowledge regarding the various algorithms used for optimization of power and area

UNIT - I	Lecture Hrs:

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT - II	Lecture Hrs:

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT - III	Lecture Hrs:

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floorplanning, wiresizing, Approximation andfitting-Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT - IV	Lecture Hrs:

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mappingfor FPGA-Automatic testgeneration-Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

UNIT - V	Lecture Hrs:

GA Routing Proceduresand Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application ofGA Standard cellplacement – GAforATG-problem encoding-fitness function-GA Vs Conventional algorithm.

Textbooks:

1.Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, DennisSylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -PinakiMazumder, E.Mrudnick, Prentice Hall,1998.

Reference Books:

1.Convex Optimization- Stephen Boyd, LievenVandenberghe, Cambridge University Press,2004

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SoC ARCHITECTURE	L	T	P	C
21D06203a		3	0	0	3
	Semester	**III**			

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

Course Outcomes (CO): Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

UNIT - I	Lecture Hrs:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II	Lecture Hrs:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III	Lecture Hrs:

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV	Lecture Hrs:

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V	Lecture Hrs:

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3.System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

AUDIT COURSE-I

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
21DAC101a		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

Course Outcomes (CO): Student will be able to

- Understand the significance of writing skills and the level of readability
- Analyze and write title, abstract, different sections in research paper
- Develop the skills needed while writing a research paper

UNIT - I	Lecture Hrs:10

1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

UNIT - II	Lecture Hrs:10

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

UNIT - III	Lecture Hrs:10

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT - IV	Lecture Hrs:9

Key skills needed for writing a Title, Abstract, and Introduction

UNIT - V	Lecture Hrs:9

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

Suggested Reading

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	DISASTER MANAGEMENT	L	T	P	C
21DAC101b		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluatedisasterriskreduction and humanitarian response policy and practice from Multiple perspectives.
- Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations
- Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches,planningand programming in different countries, particularly their home country or the countries they work in

UNIT - I

Introduction:
Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT - II

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,DroughtsandFamines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering ADisasteror Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV

Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. TechniquesofRiskAssessment,GlobalCo-OperationinRiskAssessmentand Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V

Disaster Mitigation:
Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigationand Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies
2. "'New Royal book

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Company..Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesAndReflections",PrenticeHall OfIndia, New Delhi.
3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies",Deep&Deep Publication Pvt. Ltd., New Delhi

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SANSKRITFOR TECHNICAL KNOWLEDGE	L	T	P	C
21DAC101c		2	0	0	0
	Semester	**I**			

Course Objectives: This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancientliterature

Course Outcomes (CO): Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science &technology can be understood
- Being a logical language will help to develop logic in students

UNIT - I		
Alphabets in Sanskrit,		
UNIT - II		
Past/Present/Future Tense, Simple Sentences		
UNIT - III		
Order, Introduction of roots		
UNIT - IV		
Technical information about Sanskrit Literature		
UNIT - V		
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics		

Suggested Reading

1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3.“India’s Glorious ScientificTradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi

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M.TECH. IN VLSI/VLSI DESIGN/VLSI YSTEM DESIGN

COMMON COURSE STRUCTURE & SYLLABI

AUDIT COURSE-II

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	PEDAGOGY STUDIES	L	T	P	C
21DAC201a		2	0	0	0
	Semester	II			

Course Objectives: This course will enable students:

- Reviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes (CO): Student will be able to

Students will be able to understand:

- Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidance materials best support effective pedagogy?

UNIT - I

Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories oflearning,Curriculum,Teachereducation.Conceptualframework,Research questions**.** Overview of methodology and Searching.

UNIT - II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT - III

Evidence on theeffectivenessofpedagogicalpractices,Methodologyfortheindepthstage:quality assessmen t of included studies. How can teacher education (curriculumandpracticum) andthescho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of th body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT - IV

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacherandthecommunity.Curriculumandassessment,Barrierstolearning:limitedresourcesand large class sizes

UNIT - V

Researchgapsandfuturedirections: Researchdesign**,**Contexts**,**Pedagogy**,**Teachereducation**,** Curriculum and assessment**,** Dissemination and research impact.

Suggested Reading

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof
3. Curriculum Studies, 36 (3): 361-379.

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COMMON COURSE STRUCTURE & SYLLABI

4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teachereducation research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacherpreparation count?International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
   Chavan M (2003)ReadIndia: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	STRESSMANAGEMENT BY YOGA	L	T	P	C
21DAC201b		2	0	0	0
	Semester	**II**			
Course Objectives: This course will enable students:					
• To achieve overall health of body and mind • To overcome stres					
Course Outcomes (CO): Student will be able to					
• Develop healthy mind in a healthy body thus improving social health also • Improve efficiency					
UNIT - I					
Definitions of Eight parts of yog.(Ashtanga)					
UNIT - II					
Yam and Niyam.					
UNIT - III					
Do`sand Don't'sin life. i) Ahinsa,satya,astheya,bramhacharyaand aparigrahaii) Shaucha,santosh,tapa,swadhyay,ishwarpranidhan					
UNIT - IV					
Asan and Pranayam					
UNIT - V					
i)Variousyogposesand theirbenefitsformind &body ii)Regularizationofbreathingtechniques and its effects-Types ofpranayam					
Suggested Reading					
1.'Yogic Asanas forGroupTarining-Part-I": Janardan SwamiYogabhyasiMandal, Nagpur 2."Rajayogaor conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata					

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Course Code	PERSONALITY DEVELOPMENT THROUGHLIFE ENLIGHTENMENTSKILLS	L	T	P	C
21DAC201c		2	0	0	0
	Semester	**II**			

Course Objectives: This course will enable students:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes (CO): Student will be able to

- StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achieve the highest goal in life
- The person who has studied Geetawilllead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT - I

Neetisatakam- Holistic development of personality
Verses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT - II

Neetisatakam- Holistic development of personality
Verses-52,53,59(dont's)
Verses-71,73,75,78(do's)

UNIT - III

Approach to day to day work and duties.
ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48.

UNIT - IV

Statements of basic knowledge.
ShrimadBhagwadGeeta:Chapter2-Verses 56,62,68
Chapter12 -Verses13,14,15,16,17,18
Personality of Rolemodel. Shrimad Bhagwad Geeta:

UNIT - V

Chapter2-Verses 17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

Suggested Reading

1."SrimadBhagavadGita"bySwamiSwarupanandaAdvaitaAshram(PublicationDepartment), Kolkata
2.Bhartrihari'sThree Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskrit Sansthanam, New Delhi.

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OPEN ELECTIVE

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	INDUSTRIAL SAFETY	L	T	P	C
21DOE301b		3	0	0	3
Semester		III			

Course Objectives:

- To know about Industrial safety programs and toxicology, Industrial laws , regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyse industrial hazards and its risk assessment.

Course Outcomes (CO): Student will be able to

- To list out important legislations related to health, Safety and Environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

UNIT - I Lecture Hrs:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II Lecture Hrs:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III Lecture Hrs:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working andapplications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV Lecture Hrs:

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V Lecture Hrs:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Textbooks:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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Course Code	BUSINESS ANALYTICS	L	T	P	C
21DOE301c		3	0	0	3
Semester		III			

Course Objectives:

- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

Course Outcomes (CO): Student will be able to

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT - I — Lecture Hrs:

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.
Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

UNIT - II — Lecture Hrs:

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

UNIT - III — Lecture Hrs:

Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents.Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling

UNIT - IV — Lecture Hrs:

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools

UNIT - V — Lecture Hrs:

Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

Textbooks:

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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COMMON COURSE STRUCTURE & SYLLABI

Course Code	**WASTE TO ENERGY**	**L**	**T**	**P**	**C**
21DOE301e		**3**	**0**	**0**	**3**
	Semester	**III**			

Course Objectives:

- Introduce and explain energy from waste, classification and devices to convert waste to energy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties ,bio energy system, biomass resources and their classification and biomass energy programme in India.

Course Outcomes (CO): Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion process in detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.

UNIT - I	Lecture Hrs:10

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II	Lecture Hrs:10

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT - III	Lecture Hrs:12

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

UNIT - IV	Lecture Hrs:12

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT - V	Lecture Hrs:10

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification -
Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Textbooks:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017

Reference Books:

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley

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& Sons, 1996
Online Learning Resources:
https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/ https://www.youtube.com/watch?v=x2KmjbCvKTk